LC76G Series

Reference Design

GNSS Module Series

Version: 1.1

Date: 2023-02-09

Status: Released

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

About the Document

Document Information	
Title	**LC76G Series Reference Design**
Subtitle	GNSS Module Series
Document Type	Reference Design
Document Status	Released

Revision History

Version	Date	Description
-	2022-05-11	Creation of the document
1.0	2022-07-14	First official release
1.1	2023-02-09	1. Added the applicable variant LC76G (PB). 2. Reserved the AP_REQ pin and deleted the corresponding circuit. 3. Added I2C function for LC76G (PA). 4. Added the level-shifting circuits for UART interface (Sheets 1 and 3). 5. Updated VCC power supply control circuit (Sheet 2). 6. Updated the note about supported messages for UART (Sheet 4). 7. Deleted 1PPS indication circuit. 8. Added the optional notch circuit and band-pass filter circuit to active and passive antenna reference designs, as well as the corresponding note (Sheet 5). 9. Added the SCH and PCB design checklists.

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design of Quectel LC76G GNSS module, including the design of block diagram, MCU circuit and power supply, UART level-shifting circuit, module interfaces and antenna interface. It also comprises SCH and PCB design checklists.

The LC76G series comprises three variants: LC76G (AB), LC76G (PA) and LC76G (PB)*.

1.1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	The asterisk (*) after a model indicates that the sample of the model is currently unavailable.

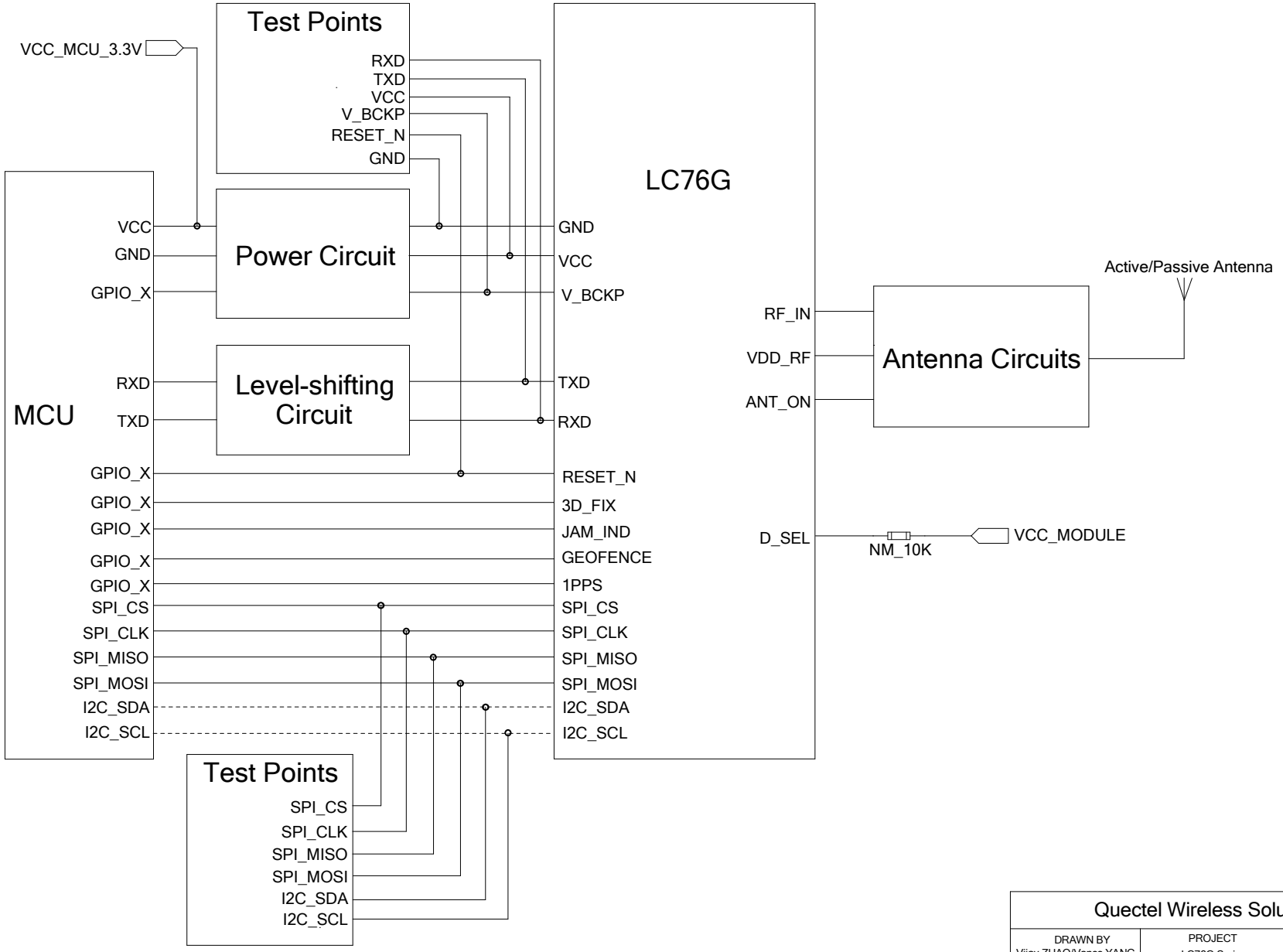
1.2. Reference Schematics and Design Checklists

The schematics and design checklists illustrated in the following pages are provided for your reference only.

NOTE

Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

Block Diagram



NOTE:

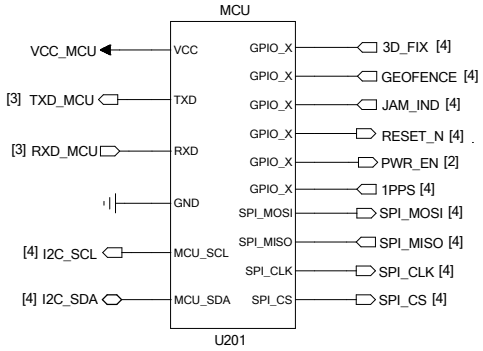
The D_SEL pin is internally pulled down by default and the UART is selected to download.

If SPI is selected to download, pull the D_SEL pin up to VCC externally with a 10 kΩ resistor.

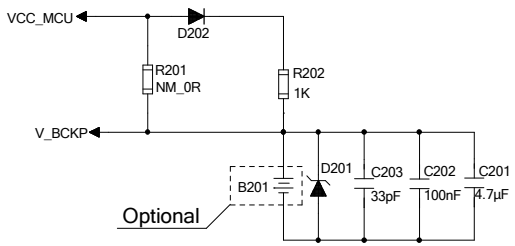
Quectel Wireless Solutions		
DRAWN BY Vijay ZHAO/Vance YANG	PROJECT LC76G Series	TITLE Reference Design
CHECKED BY Storm BAO	SIZE A2	VER 1.1
	SHEET 1 OF 5	DATE 2023/2/9

MCU Circuit and Power Supply

MCU Circuit



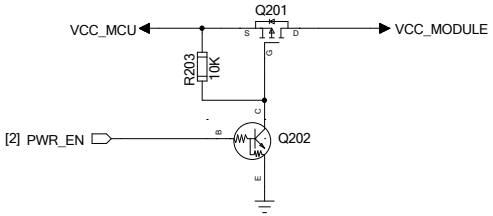
V_BCKP Power Supply Circuit



NOTE:

1. The rechargeable battery (B201) is optional:
   For LC76G (AB, PA), it is recommended to use the above circuit.
   For LC76G (PB), when the VCC_MCU is 1.8 V voltage, the B201 and D202 are omitted and it is recommended to use a 1.8 V power supply in the above circuit.
2. V_BCKP must be powered before or simultaneously with the VCC_MODULE.
3. It is recommended to control the V_BCKP of the module via MCU to restart when the module enters abnormal state.
4. For more information, see *Quectel_LC76G_Series_Hardware_Design*.

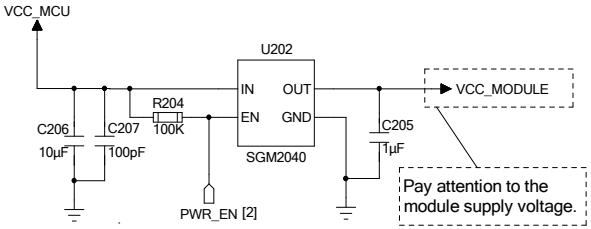
LC76G (AB, PA) Power Supply Control Circuit



NOTE:

1. This circuit can be used to control the VCC power supply of the LC76G (AB, PA) module through MCU.
2. Ensure the VCC_MODULE is controlled by MCU to save power or restart the module when the module enters abnormal state.

LC76G (PB) Power Supply Control Circuit



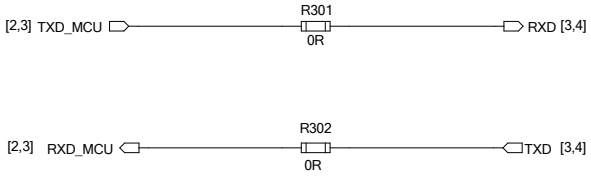
NOTE:

1. It is recommended to use the LDO with 1.8 V output voltage.
2. Ensure the VCC_MODULE is controlled by MCU to save power or restart the module when the module enters abnormal state.

Quectel Wireless Solutions		
DRAWN BY Vijay ZHAO/Vance YANG	PROJECT LC76G Series	TITLE Reference Design
CHECKED BY Storm BAO	SIZE A2	VER 1.1
	SHEET 2 OF 5	DATE 2023/2/9

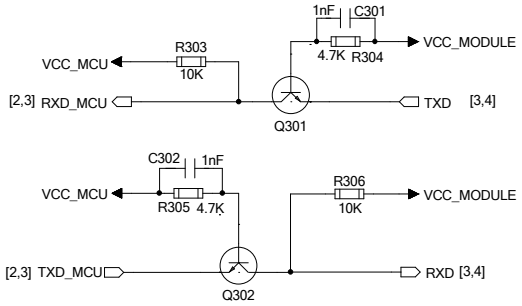
UART Level-shifting Circuit

LC76G (AB, PA) – Resistor Circuit Solution



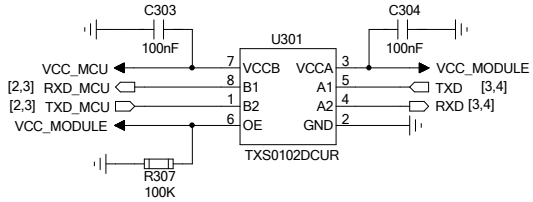
NOTE:
1. R301 and R302 are reserved for debugging the waveform of UART.
2. The above circuit is designed when UART voltage of MCU is consistent with that of the module.

LC76G (PB) – Transistor Solution



NOTE:
The above circuit is designed to achieve the level shifting between VCC_MCU and VCC_MODULE, and block the leakage current from a power-on device to a power-off device.

LC76G (PB) – IC Solution

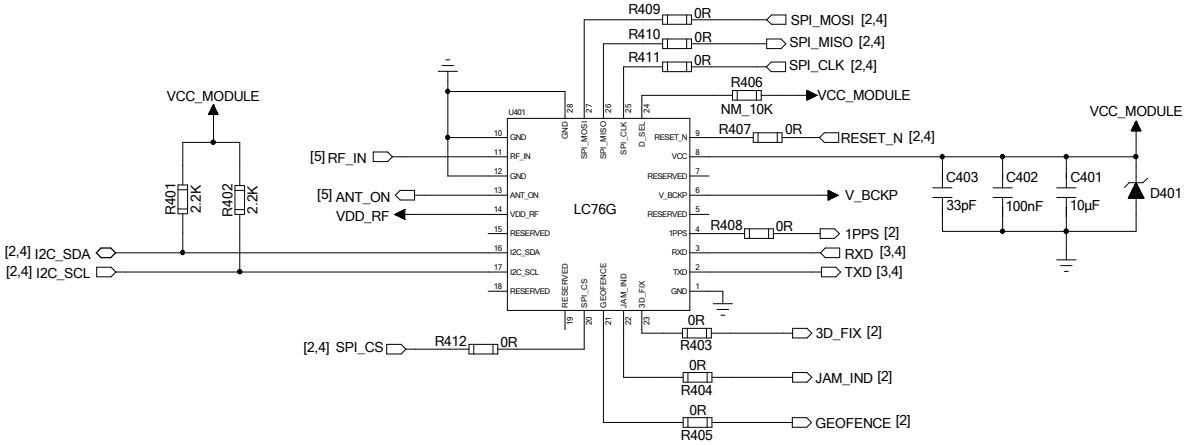


NOTE:
1. The IC solution generally requires VCCA ≤ VCCB. Please pay attention to the voltage relationship when using it.
2. The above circuit is designed to achieve the level shifting between VCC_MCU and VCC_MODULE.

Quectel Wireless Solutions		
DRAWN BY Vijay ZHAO/Vance YANG	PROJECT LC76G Series	TITLE Reference Design
CHECKED BY Storm BAO	SIZE A2	VER 1.1
	SHEET 3 OF 5	DATE 2023/2/9

Module Interfaces

Module Interfaces

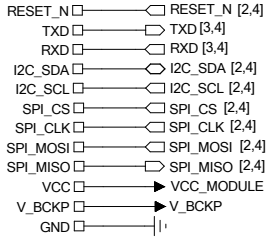


Module / Voltage	LC76G (AB)	LC76G (PA)	LC76G (PB)
VCC_MODULE	2.55-3.6 V	2.55-3.6 V	1.75-1.98 V
I/O Level	Same as VCC	Same as VCC	Same as VCC
V_BCKP	1.65-3.6 V	1.65-3.6 V	1.65-3.6 V

NOTE:

1. The UART interface can be used for RTCM and standard NMEA message output, PQTM/PAIR message and binary data input/output, and firmware upgrade.
2. The power supply design must meet the sequence requirements in hardware design. For more information, see *Quectel_LC76G_Series_Hardware_Design*.
3. A level-shifting circuit must be used when the I/O voltage of MCU is not matched with that of the module.
4. Externally pull D_SEL up with a 10 kΩ resistor for SPI to download.
5. The RESET_N pin is internally pulled up to 1.8 V; the pin must be connected so that it can be used to reset the module if the module enters an abnormal state.

Test Points



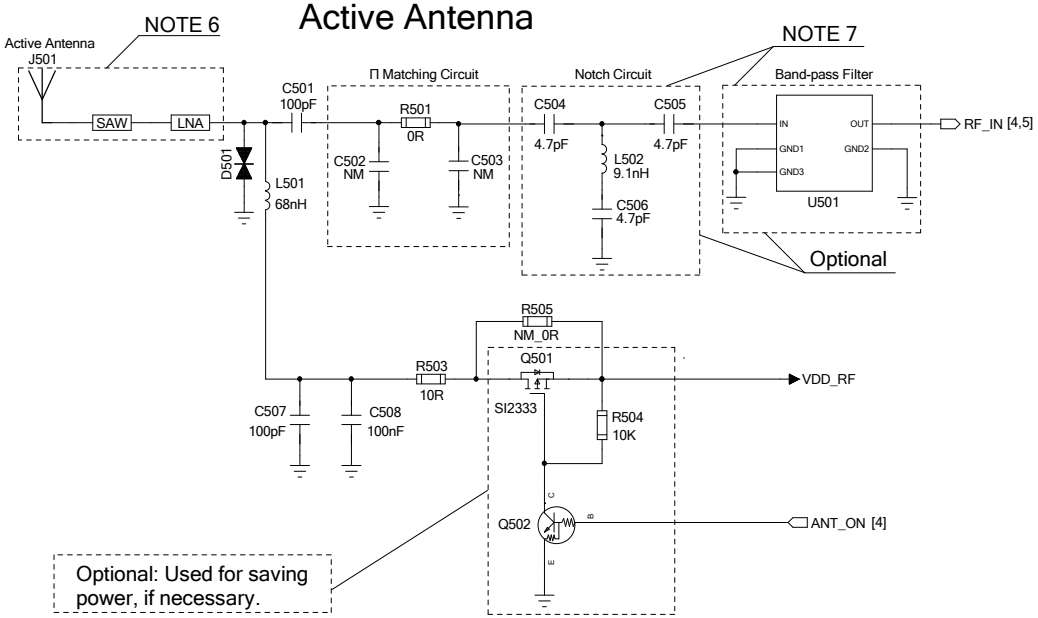
NOTE:

Reserve test points for debugging the module.

Quectel Wireless Solutions		
DRAWN BY Vijay ZHAO/Vance YANG	PROJECT LC76G Series	TITLE Reference Design
CHECKED BY Storm BAO	SIZE A2	VER 1.1
	SHEET 4 OF 5	DATE 2023/2/9

Antenna Interface

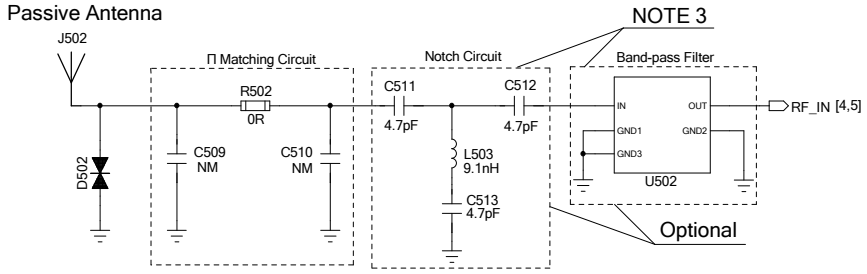
Active Antenna



NOTE:

1. C502, C503 and R501 form a Π matching circuit for antenna impedance modification. By default, R501 is 0 Ω, and C502 and C503 are not mounted.
2. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
3. D501 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
4. L501 is used for preventing the RF signal from leaking into the VDD_RF and preventing noise propagation from the VDD_RF to the antenna.
5. The resistor R503 is used for protecting the module in case the active antenna is short-circuited to the ground plane.
6. In the internal framework of active antenna, it is recommended to place the SAW filter in front of the LNA, which can be used to further reduce the impact of out-of-band signals on GNSS module when there is a complex electromagnetic environment around the module.
7. In a complex electromagnetic environment, a notch circuit and a band-pass filter circuit are optional and recommended to be added to further reduce the impact of out-of-band signals on GNSS module. They should be placed close to the RF_IN pin during PCB design.
8. For more informaton, see *Quectel_LC76G_Series_Hardware_Design.*

Passive Antenna



NOTE:

1. C509, C510 and R502 form a Π matching circuit for antenna impedance modification. By default, R502 is 0 Ω, and C509 and C510 are not mounted.
2. D502 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
3. In a complex electromagnetic environment, a notch circuit and a band-pass filter circuit are optional and recommended to be added to further reduce the impact of out-of-band signals on GNSS module. They should be placed close to the RF_IN pin during PCB design.
4. For more information, see *Quectel_LC76G_Series_Hardware_Design.*

Quectel Wireless Solutions		
DRAWN BY Vijay ZHAO/Vance YANG	PROJECT LC76G Series	TITLE Reference Design
CHECKED BY Storm BAO	SIZE A2	VER 1.1
	SHEET 5 OF 5	DATE 2023/2/9

Table 1: SCH Design Checklist

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
1	GND	Reference ground of the module. The GND pin must be connected to ground.				
2	TXD	Connect to MCU through 0 Ω resistors or a level-shifting circuit. Reserve test points.				
3	RXD					
4	1PPS	Connect to the GPIO of the MCU. If unused, leave the pin N/C (not connected).				
5	RESERVED	The RESERVED pin must be left floating.				
6	V_BCKP	1. It is recommended to place a TVS, and a combination of a 4.7 μF, a 100 nF and a 33 pF decoupling capacitor near the V_BCKP pin. 2. Ensure that V_BCKP is controlled by MCU. 3. Reserve a test point. 4. V_BCKP must be connected to power supply for startup, and it should always be powered if hot (warm) start is needed.				
7	RESERVED	The RESERVED pin must be left floating.				
8	VCC	1. It is recommended to place a TVS, and a combination of a 10 μF, a 100 nF and a 33 pF decoupling capacitor near the VCC pin. 2. Ensure that VCC is controlled by MCU. 3. Reserve a test point.				
9	RESET_N	Connect a 0 Ω resistor in series and the pin must be controlled by an external MCU. Reserve a test point.				
10	GND	Reference ground of the module. The GND pin must be connected to ground.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
11	RF_IN	1. π matching circuit must be added for impedance modification. 2. In a complex electromagnetic environment, a notch circuit and a band-pass filter circuit must be added to reduce the impact of out-of-band signals interference. 3. It is recommended to select an ESD protection device with junction capacitance lower than 0.6 pF. 4. The inductor used in the power supply circuit of the active antenna is at least 68 nH and the inductor is placed so that its pad is part of the RF line.				
12	GND	Reference ground of the module. The GND pin must be connected to ground.				
13	ANT_ON	ANT_ON is connected to the transistor's base to control the power supply of VDD_RF for external active antenna or LNA.				
14	VDD_RF	Used to supply power for external active antenna or LNA.				
15	RESERVED	The RESERVED pin must be left floating.				
16	I2C_SDA	1. The pins are pulled up externally to VCC with a 2.2 kΩ resistor respectively. 2. Connect them to MCU with a level-shifting circuit. Reserve test points. If unused, leave the pins N/C.				
17	I2C_SCL					
18	RESERVED	The RESERVED pin must be left floating.				
19	RESERVED	The RESERVED pin must be left floating.				
20	SPI_CS	Connect to MCU and reserve a test point; if unused, leave the pin N/C.				
21	GEOFENCE	Connect to the GPIO of the MCU. If unused, leave the pin N/C.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
22	JAM_IND	Connect to the GPIO of the MCU. If unused, leave the pin N/C.				
23	3D_FIX	Connect to the GPIO of the MCU. If unused, leave the pin N/C.				
24	D_SEL	Connect a 10 kΩ resistor in series to VCC. The resistor is not mounted by default.				
25	SPI_CLK	Connect to MCU and reserve a test point; if unused, leave the pin N/C.				
26	SPI_MISO	Connect to MCU and reserve a test point; if unused, leave the pin N/C.				
27	SPI_MOSI	Connect to MCU and reserve a test point; if unused, leave the pin N/C.				
28	GND	Reference ground of the module. The GND pin must be connected to ground.				

NOTE

1. All GND pins must be connected to ground and reserved a GND test point; all RESERVED pins must be left floating.
2. Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.

Table 2: PCB Design Checklist

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
1	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
2	TXD	Surround the signal traces with ground. Keep the routing short and away from interference sources.				
3	RXD					
4	1PPS	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
5	RESERVED	/				
6	V_BCKP	1. The power supply first passes through the TVS, and then through the subsequent components. 2. The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements. 3. The routing width of the power supply is at least 1 mm per ampere. The longer the routing, the wider it should be. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated.				
7	RESERVED	/				
8	VCC	1. The power supply first passes through the TVS, and then through the subsequent components. 2. The capacitors are placed near the power supply pin in descending order of capacitance. At least one GND via must be placed near the grounded end of the capacitor. If needed, there should be more than one GND via to meet the requirements.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
		3. The routing width of the power supply is at least 1 mm per ampere. The longer the routing, the wider it should be. The power routing and sensitive signal routings (with Clock, USB, MIPI, RF, etc.) must be isolated.				
9	RESET_N	Surround the RESET_N signal trace with ground, and avoid routing near the strong interference signals.				
10	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
11	RF_IN	1. The characteristic impedance of the RF signal line(s) is kept at 50 Ω, and the RF trace is as short and straight as possible, with smooth lines (without bumps, with consistent geometry–it would be ideal for the footprints to be blended into the RF trace, with curved rather than sharp angles). 2. Ensure that there are no vias in the RF signal path. 3. Ensure that RF signal path is surrounded by ground. 4. RF signal line(s) and GNSS antenna are kept away from noise sources such as MCU(s), crystal(s) and other RF antenna(s).				
12	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				
13	ANT_ON	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
14	VDD_RF	Power routing should be surrounded by GND and avoid being parallel with other line(s).				
15	RESERVED	/				
16	I2C_SDA	1. Surround the signal traces with ground.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
17	I2C_SCL	2. Keep the routing short and stay away from distractions.				
18	RESERVED	/				
19	RESERVED	/				
20	SPI_CS	1. Surround the signal trace with ground. 2. Keep the routing short and stay away from distractions.				
21	GEOFENCE	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
22	JAM_IND	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
23	3D_FIX	1. Surround the signal trace with ground. 2. Avoid routing near strong interference signals; avoid acute angles and right angles in trace routing.				
24	D_SEL	1. Surround the signal traces with ground. 2. Place the pull-up resistor close to the pin.				
25	SPI_CLK	1. Surround the signal trace with ground. 2. Keep the routing short and stay away from distractions.				
26	SPI_MISO	1. Surround the signal trace with ground. 2. Keep the routing short and stay away from distractions.				
27	SPI_MOSI	1. Surround the signal trace with ground. 2. Keep the routing short and stay away from distractions.				

Pin No.	Pin Name	Checklist	Result			Comment
			Pass	Fail	N/A	
28	GND	1. Confirm that there are no isolated shapes in the ground layer. 2. Module GND pads must be completely covered by the ground plane.				

NOTE

Quectel also provides design review services. It is strongly recommended that you submit your schematics and PCB designs to Quectel Technical Support for a formal review.