

SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

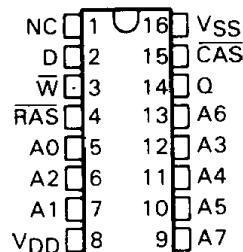
JULY 1985 — REVISED MAY 1988

- 65,536 × 1 Organization
- Single 5-V Supply ($\pm 10\%$ Tolerance)
- Upward Pin Compatible with '4116 (16K Dynamic RAM)
- Available Temperature Ranges with MIL-STD-883C High-Reliability Class B Processing:
 - S . . . -55°C to 110°C
 - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with Early Write Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
 - Operating . . . 125 mW (Typ)
 - Standby . . . 17.5 mW (Typ)
- Performance Ranges:

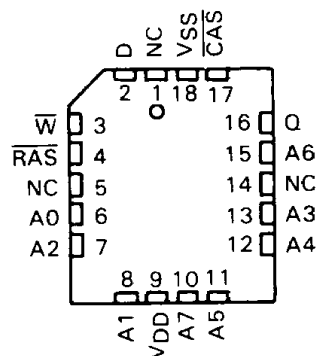
	ACCESS TIME (MAX)	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ OR WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	326 ns	345 ns

- SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0-A7	Address Inputs
CAS	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
RAS	Row-Address Strobe
VDD	5-V Supply
VSS	Ground
W	Write Enable

description

The SMJ4164 is a Military high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4164 features $\overline{\text{RAS}}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 125 mW typical operating and 17.5 mW typical standby.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Copyright © 1985, Texas Instruments Incorporated

14-511

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The SMJ4164 is offered in a 16-pin dual-in-line ceramic sidebrazed package (JD suffix) and in a leadless ceramic chip carrier package (FG suffix). The JD package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers, whereas the FG package is intended for surface mounting on solder lands on 1,27-mm (0.050-inch) centers. The FG package is a three-layer, 18-pad, rectangular ceramic chip carrier with dimensions of 7,37 × 10,8 × 1,65 mm (0.290 × 0.425 × 0.065 inches).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{\text{RAS}}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{\text{CAS}}$). All addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{CAS}}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through the write-enable ($\overline{\text{W}}$) input. A logic high on the $\overline{\text{W}}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{\text{W}}$ goes low prior to $\overline{\text{CAS}}$, data-out will remain in the high-impedance state for the entire cycle, permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{\text{CAS}}$ will already be low, thus the data will be strobed in by $\overline{\text{W}}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{CAS}}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{\text{CAS}}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{\text{CAS}}$ is low; $\overline{\text{CAS}}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{\text{CAS}}$ is applied, the $\overline{\text{RAS}}$ -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed. $\overline{\text{CAS}}$ can remain high (inactive) for this refresh sequence to conserve power.

SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

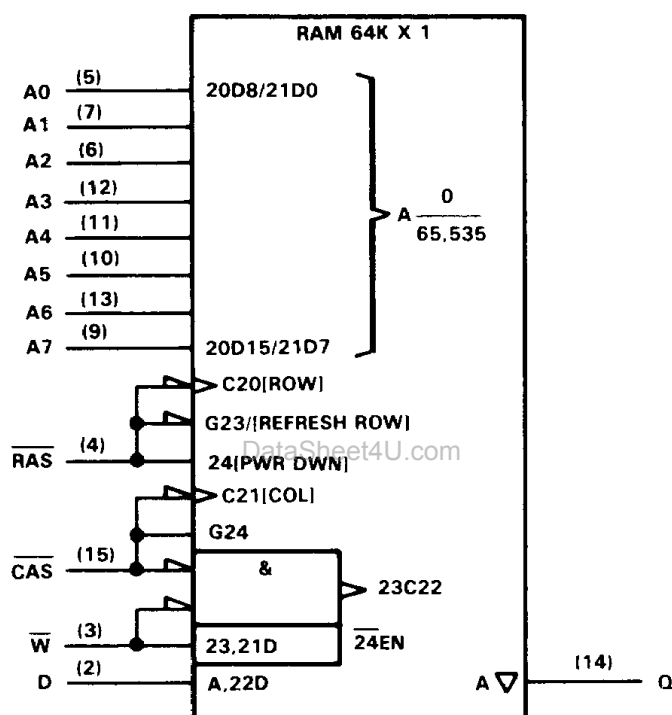
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{\text{RAS}}$ are applied to multiple 64K RAMs. $\overline{\text{CAS}}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{\text{RAS}}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{\text{RAS}}$ cycles before proper device operation is achieved.

logic symbol†

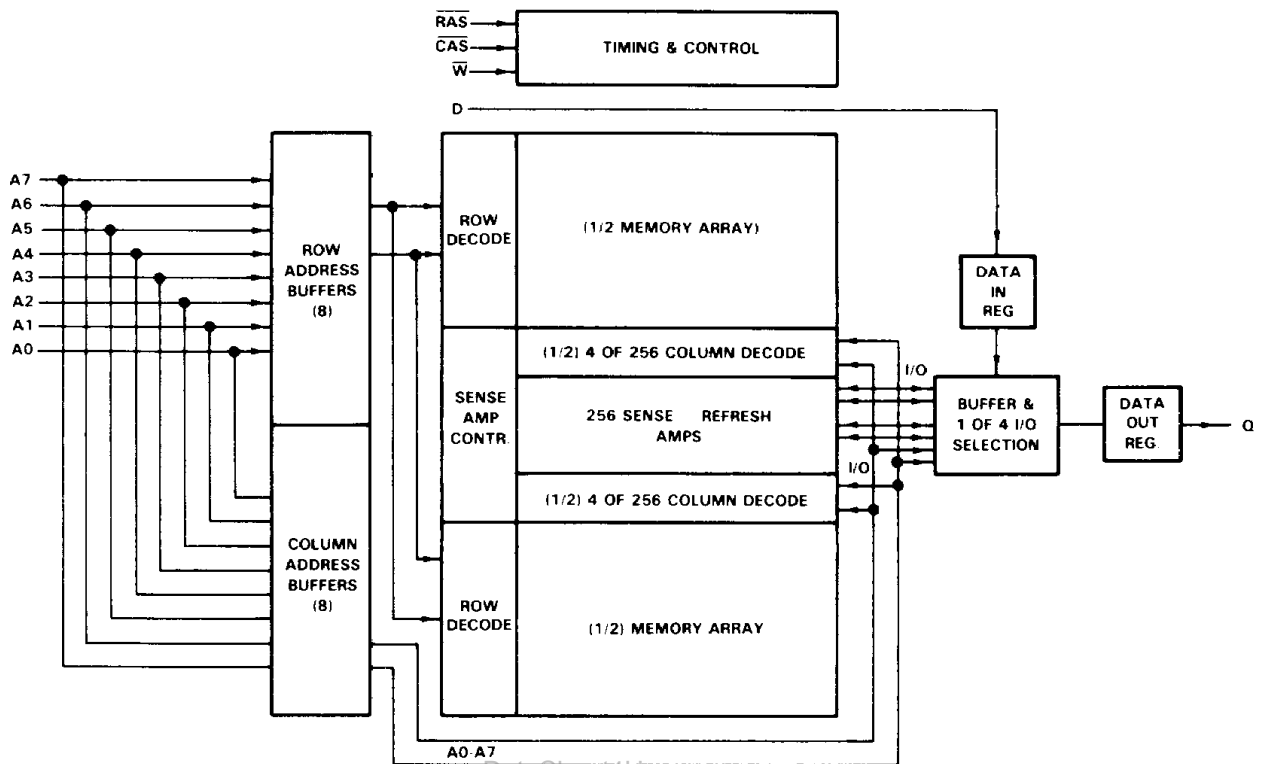


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the dual-in-line package.

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)[†]

Voltage on any pin except V _{DD} and data out (see Note 1)	-1.5 V to 10 V
Voltage on V _{DD} supply and data out with respect to V _{SS}	-1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	-55 °C
L version	0 °C
Operating case temperature: S version	110 °C
L version	70 °C
Storage temperature range	-65 °C to 150 °C

[†]Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

recommended operating conditions

		S VERSION			L VERSION			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{DD}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{SS}	Supply voltage	0			0			V
V _{IH}	High-level input voltage	2.4			V _{CC} +0.3			V
V _{IL}	Low-level input voltage (see Notes 3 and 4)	-0.6			0.8			V
T _A	Operating free-air temperature	-55			0			°C
T _C	Operating case temperature	110			70			°C

- NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions must comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SMJ4164-12			SMJ4164-15			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V _{OH}	High-level output voltage I _{OH} = -5 mA	2.4			2.4			V
V _{OL}	Low-level output voltage I _{OL} = 4.2 mA			0.4			0.4	V
I _I	Input current (leakage) V _I = 0 V to 5.8 V, V _{DD} = 5.5 V All outputs open			± 10			± 10	μA
I _O	Output current (leakage) V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, $\overline{\text{CAS}}$ high			± 10			± 10	μA
I _{DD1} [‡]	Average operating current during read or write cycle t _c = minimum cycle, All outputs open		40	48		35	45	mA
I _{DD2} [§]	Standby current After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open		3.5	5		3.5	5	mA
I _{DD3} [†]	Average refresh current t _c = minimum cycle, $\overline{\text{CAS}}$ high and $\overline{\text{RAS}}$ cycling, All outputs open		28	40		25	37	mA
I _{DD4}	Average page-mode current t _{c(P)} = minimum cycle, $\overline{\text{RAS}}$ low and $\overline{\text{CAS}}$ cycling, All outputs open		28	40		25	37	mA

[†]All typical values are at T_C = 25°C and nominal supply voltages.

[‡]Additional information on last page of data sheet.

[§]V_{IL} ≤ -0.6 V.



POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

14-515

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SMJ4164-20			UNIT
		MIN	TYP [†]	MAX	
V _{OH}	High-level output voltage	I _{OH} = -5 mA			V
V _{OL}	Low-level output voltage	I _{OL} = 4.2 mA			V
I _I	Input current (leakage)	V _I = 0 V to 5.8 V, V _{DD} = 5.5 V, Output = open			μA
I _O	Output current (leakage)	V _O = 0.4 V to 5.5 V, V _{DD} = 5 V, CAS high			μA
I _{DD1} [‡]	Average operating current during read or write cycle	t _C = minimum cycle All outputs open			mA
I _{DD2} [§]	Standby current	After 1 memory cycle, RAS and CAS high, All outputs open			mA
I _{DD3} [‡]	Average refresh current	t _C = minimum cycle, CAS high and RAS cycling, All outputs open			mA
I _{DD4}	Average page-mode current	t _{C(P)} = minimum cycle, RAS low and CAS cycling, All outputs open			mA

[†]All typical values are at T_C = 25°C and nominal supply voltages.

[‡]Additional information on last page of data sheet.

[§]V_{IL} > -0.6 V.

capacitance over recommended supply voltage range and recommended temperature range, f = 1 MHz[†]

PARAMETER	SMJ4164		UNIT	
	TYP [†]	MAX		
C _{i(A)}	Input capacitance, address inputs	4	7	pF
C _{i(D)}	Input capacitance, data input	4	7	pF
C _{i(RC)}	Input capacitance, strobe inputs	8	10	pF
C _{i(W)}	Input capacitance, write enable input	8	10	pF
C _O	Output capacitance	5	8	pF

[†]All typical values are at T_C = 25°C and nominal supply voltages.

[‡]These parameters are guaranteed but not tested.

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from \overline{CAS}			70		85	ns
$t_{a(R)}$	Access time from \overline{RAS}			120		150	ns
$t_{dis(CH)}$	Output disable time after \overline{CAS} high		0	40	0	40	ns

PARAMETER	TEST CONDITIONS	ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{a(C)}$	Access time from \overline{CAS}			135	ns
$t_{a(R)}$	Access time from \overline{RAS}			200	ns
$t_{dis(CH)}$	Output disable time after \overline{CAS} high		0	50	ns

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

timing requirements over recommended supply voltage range and recommended operating temperature range

PARAMETER	ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(P)}$ Page-mode cycle time	tpc	130		160		ns
$t_{c(rd)}$ Read cycle time [†]	tRC	230		260		ns
$t_{c(W)}$ Write cycle time	tWC	230		260		ns
$t_{c(rdW)}$ Read-write/read-modify-write cycle time	tRWC	260		285		ns
$t_w(CH)$ Pulse duration, \overline{CAS} high (precharge time) [‡]	tCP	50		50		ns
$t_w(CL)$ Pulse duration, \overline{CAS} low [§]	tCAS	70	10,000	85	10,000	ns
$t_w(RH)$ Pulse duration, \overline{RAS} high (precharge time)	tRP	80		100		ns
$t_w(RL)$ Pulse duration, \overline{RAS} low [¶]	tRAS	120	10,000	150	10,000	ns
$t_w(W)$ Write pulse duration	tWP	40		45		ns
$t_{su(CA)}$ Column-address setup time	tASC	-5		-5		ns
$t_{su(RA)}$ Row-address setup time	tASR	0		0		ns
$t_{su(D)}$ Data setup time	tDS	0		0		ns
$t_{su(rd)}$ Read-command setup time	tRCS	0		0		ns
$t_{su(WCH)}$ Write-command setup time before \overline{CAS} high	tCWL	50		50		ns
$t_{su(WRH)}$ Write-command setup time before \overline{RAS} high	tRWL	50		50		ns
$t_h(CLCA)$ Column-address hold time after \overline{CAS} low	tCAH	40		45		ns
$t_h(RA)$ Row-address hold time	tRAH	15		20		ns
$t_h(RLCA)$ Column-address hold time after \overline{RAS} low	tAR	85		95		ns
$t_h(CLD)$ Data hold time after \overline{CAS} low	tDHC	40		45		ns
$t_h(RLD)$ Data hold time after \overline{RAS} low	tDHR	85		95		ns
$t_h(WLD)$ Data hold time after \overline{W} low	tDHW	40		45		ns
$t_h(CHrd)$ Read-command hold time after \overline{CAS} high	tRCH	0		0		ns
$t_h(RHrd)$ Read-command hold time after \overline{RAS} high	tRRH	5		5		ns
$t_h(CLW)$ Write-command hold time after \overline{CAS} low	tWCH	40		45		ns
$t_h(RLW)$ Write-command hold time after \overline{RAS} low	tWCR	85		95		ns
t_{RLCH} Delay time, \overline{RAS} low to \overline{CAS} high	tCSH	120		150		ns
t_{CHRL} Delay time, \overline{CAS} high to \overline{RAS} low	tCRP	0		0		ns
t_{CLRH} Delay time, \overline{CAS} low to \overline{RAS} high	tRSH	70		85		ns

Continued next page.

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns. The recommended rise and fall times for the \overline{CAS} and \overline{RAS} inputs are a minimum of 3 ns and a maximum of 50 ns.

[‡]Page-mode only.

[§]In a read-modify-write cycle, tCLWL and t_{su}(WCH) must be observed. Depending on the user's transition times, this may require additional \overline{CAS} low time ($t_w(CL)$). This applies to page-mode read-modify-write also.

[¶]In a read-modify-write cycle, tRLWL and t_{su}(WRH) must be observed. Depending on the user's transition times, this may require additional \overline{RAS} low time ($t_w(RL)$).

^{||}These parameters are guaranteed but not tested.

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

PARAMETER		ALT. SYMBOL	SMJ4164-12		SMJ4164-15		UNIT
			MIN	MAX	MIN	MAX	
t_{CLWL}	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, \overline{RAS} low to \overline{CAS} low (maximum value specified only to guarantee access time)	t_{RCD}	15	45	20	50	ns
t_{RLWL}	Delay time, \overline{RAS} low to \overline{W} low (read-modify-write cycle only)	t_{RWD}	85		100		ns
t_{WLCL}	Delay time, \overline{W} low to \overline{CAS} low (early write cycle)	t_{WCS}	-5		-5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

timing requirements over recommended supply voltage range and recommended operating temperature range (continued)

PARAMETER		ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time [†]	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_w(CH)$	Pulse duration, \overline{CAS} high (precharge time) [‡]	t_{CP}	80		ns
$t_w(CL)$	Pulse duration, \overline{CAS} low [§]	t_{CAS}	135	10,000	ns
$t_w(RH)$	Pulse duration, \overline{RAS} high (precharge time)	t_{RP}	120		ns
$t_w(RL)$	Pulse duration, \overline{RAS} low [¶]	t_{RAS}	200	10,000	ns
$t_w(W)$	Write pulse duration	t_{WP}	55		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	-5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before \overline{CAS} high	t_{CWL}	80		ns
$t_{su(WRH)}$	Write-command setup time before \overline{RAS} high	t_{RWL}	80		ns
$t_h(CLCA)$	Column-address hold time after \overline{CAS} low	t_{CAH}	55		ns
$t_h(RA)$	Row-address hold time	t_{RAH}	25		ns
$t_h(RLCA)$	Column-address hold time after \overline{RAS} low	t_{AR}	140		ns
$t_h(CLD)$	Data hold time after \overline{CAS} low	t_{DHC}	80		ns
$t_h(RLD)$	Data hold time after \overline{RAS} low	t_{DHR}	145		ns

Continued next page.

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns. The recommended rise and fall times for the \overline{CAS} and \overline{RAS} inputs are a minimum of 3 ns and a maximum of 50 ns.

[‡]Page-mode only.

[§]In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional \overline{CAS} low time ($t_w(CL)$). This applies to page-mode read-modify-write also.

[¶]In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional \overline{RAS} low time ($t_w(RL)$).


**TEXAS
INSTRUMENTS**

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

14-519

SMJ4164

65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

timing requirements over recommended supply voltage range and recommended operating temperature range (concluded)

PARAMETERS		ALT. SYMBOL	SMJ4164-20		UNIT
			MIN	MAX	
$t_{h(WLD)}$	Data hold time after \overline{W} low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after \overline{CAS} high ¹	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after \overline{RAS} high ¹	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after \overline{CAS} low	t_{WCH}	80		ns
$t_{h(RLW)}$	Write-command hold time after \overline{RAS} low	t_{WCR}	145		ns
t_{RLCH}	Delay time, \overline{RAS} low to \overline{CAS} high	t_{CSH}	200		ns
t_{CHRL}	Delay time, \overline{CAS} high to \overline{RAS} low	t_{CRP}	0		ns
t_{CLRHL}	Delay time, \overline{CAS} low to \overline{RAS} high	t_{RSH}	135		ns
t_{CLWL}	Delay time, \overline{CAS} low to \overline{W} low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, \overline{RAS} low to \overline{CAS} low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, \overline{RAS} low to \overline{W} low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, \overline{W} low to \overline{CAS} low (early write cycle)	t_{WCS}	-5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

¹These parameters are guaranteed but not tested.

PARAMETER MEASUREMENT INFORMATION

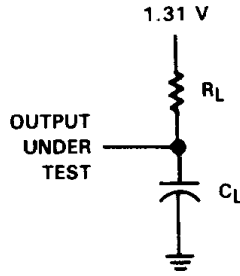
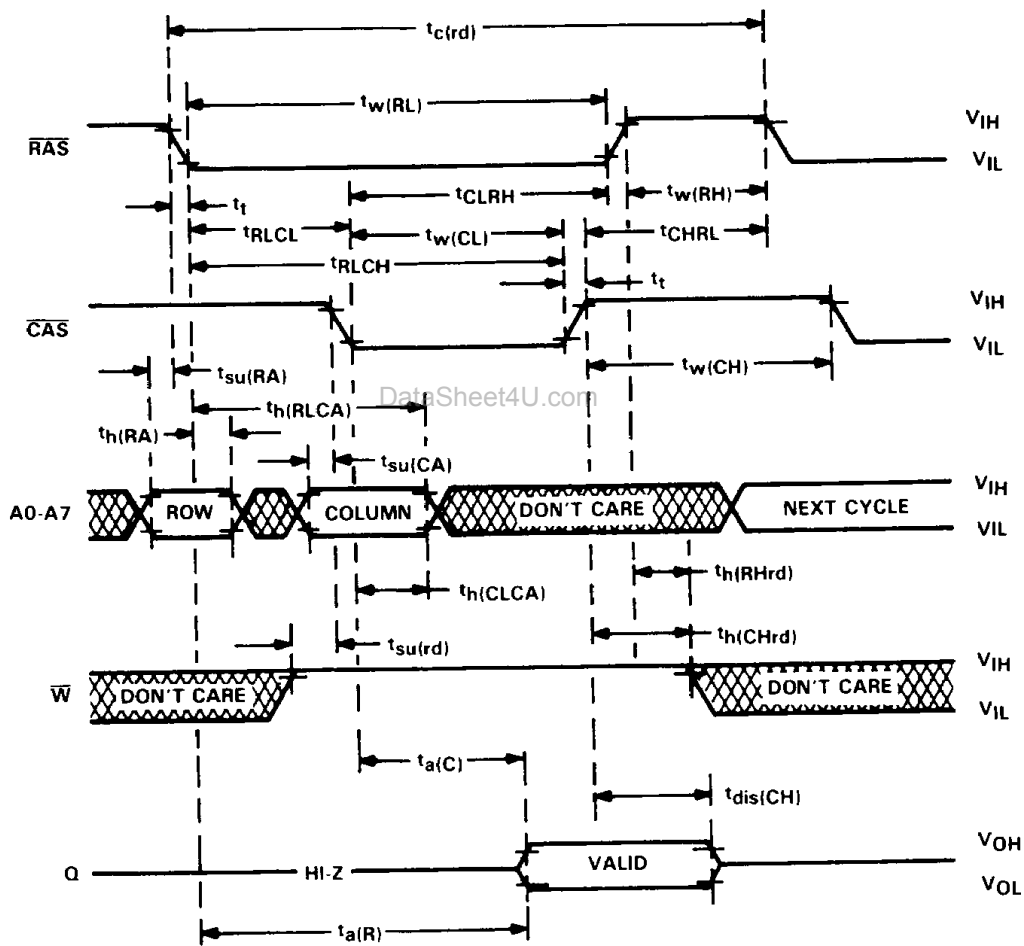


FIGURE 1. LOAD CIRCUIT

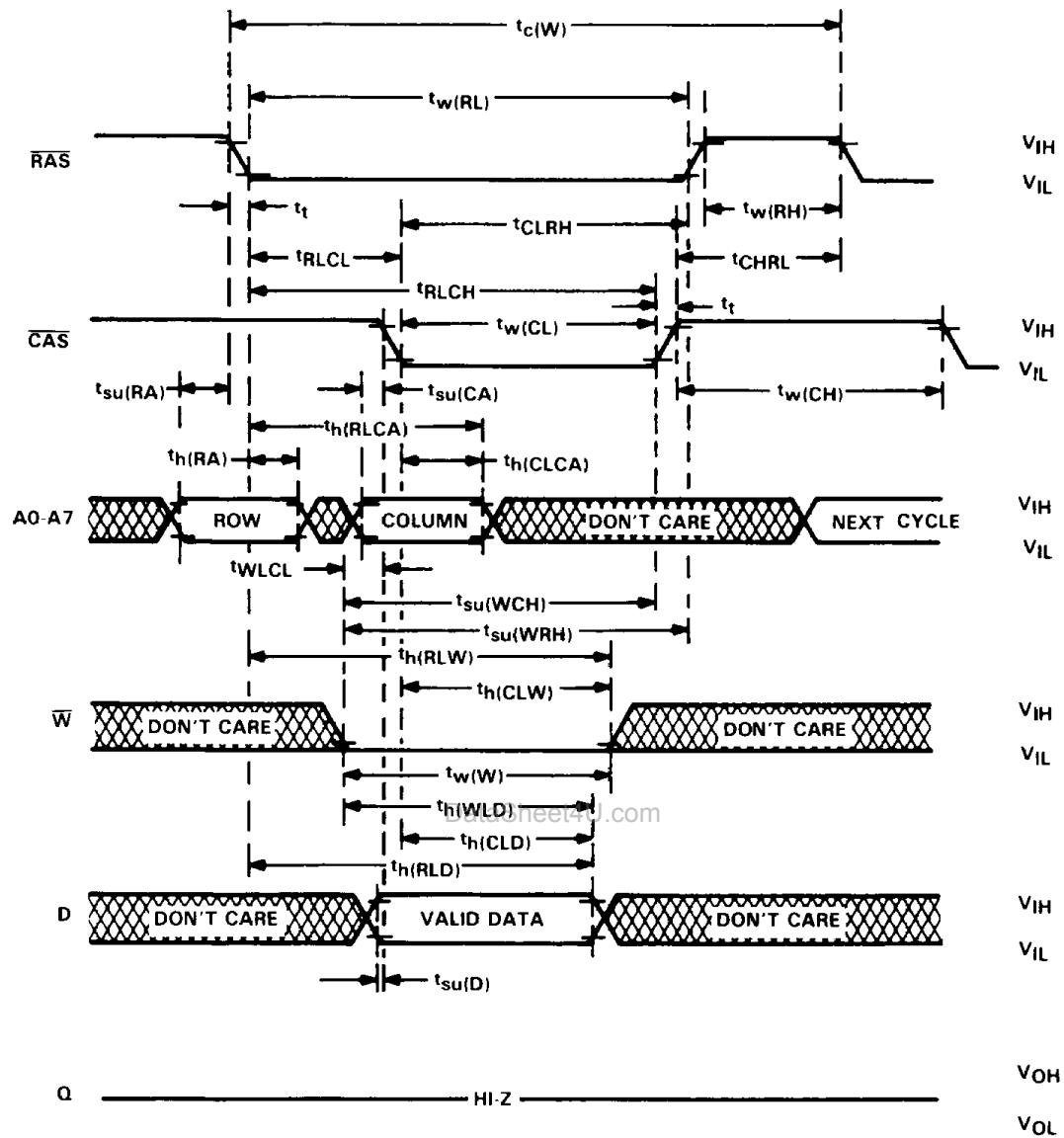
read cycle timing



POST OFFICE BOX 225012 • DALLAS, TEXAS 75285

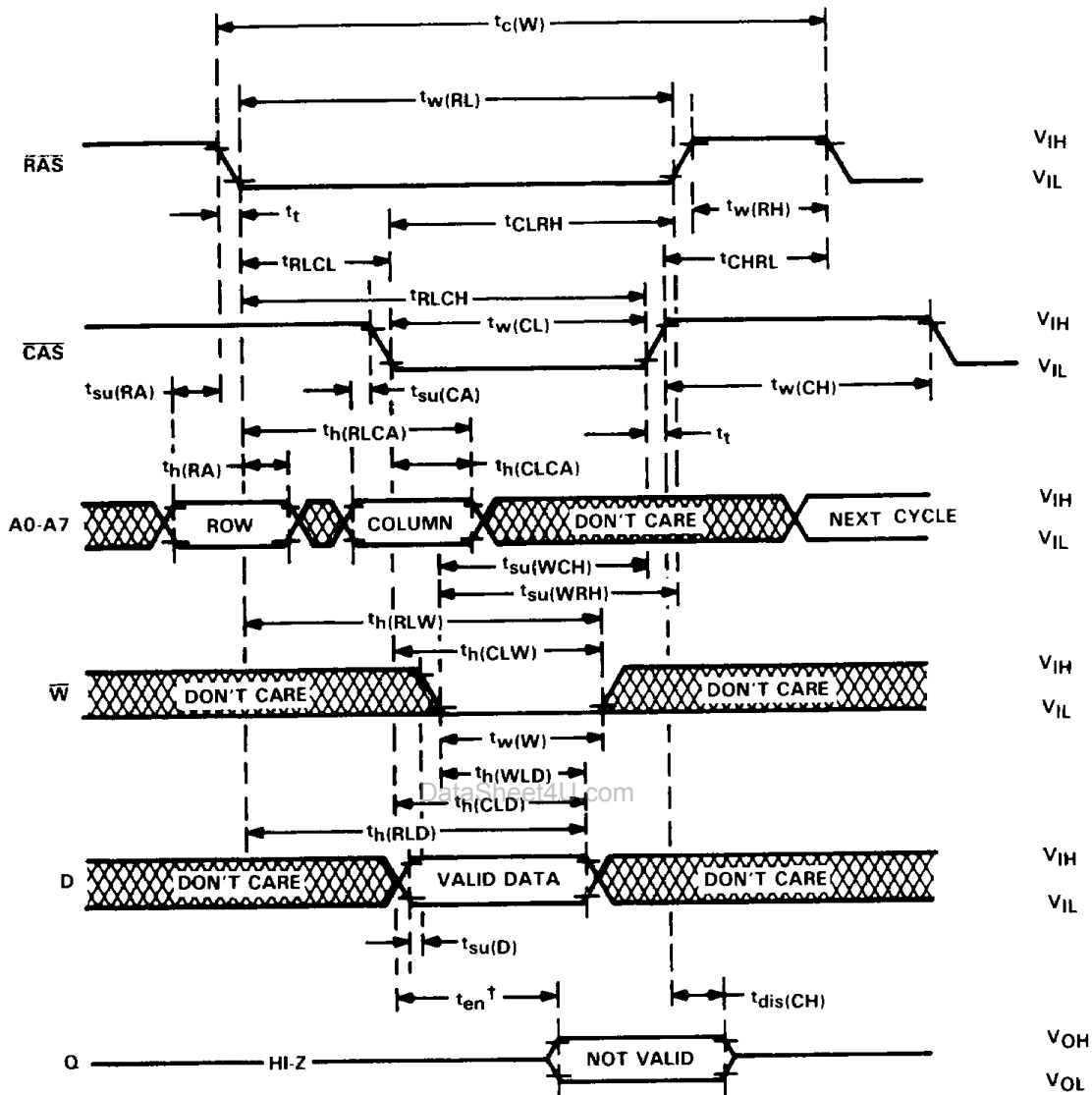
SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

early write cycle timing



SMJ4164
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

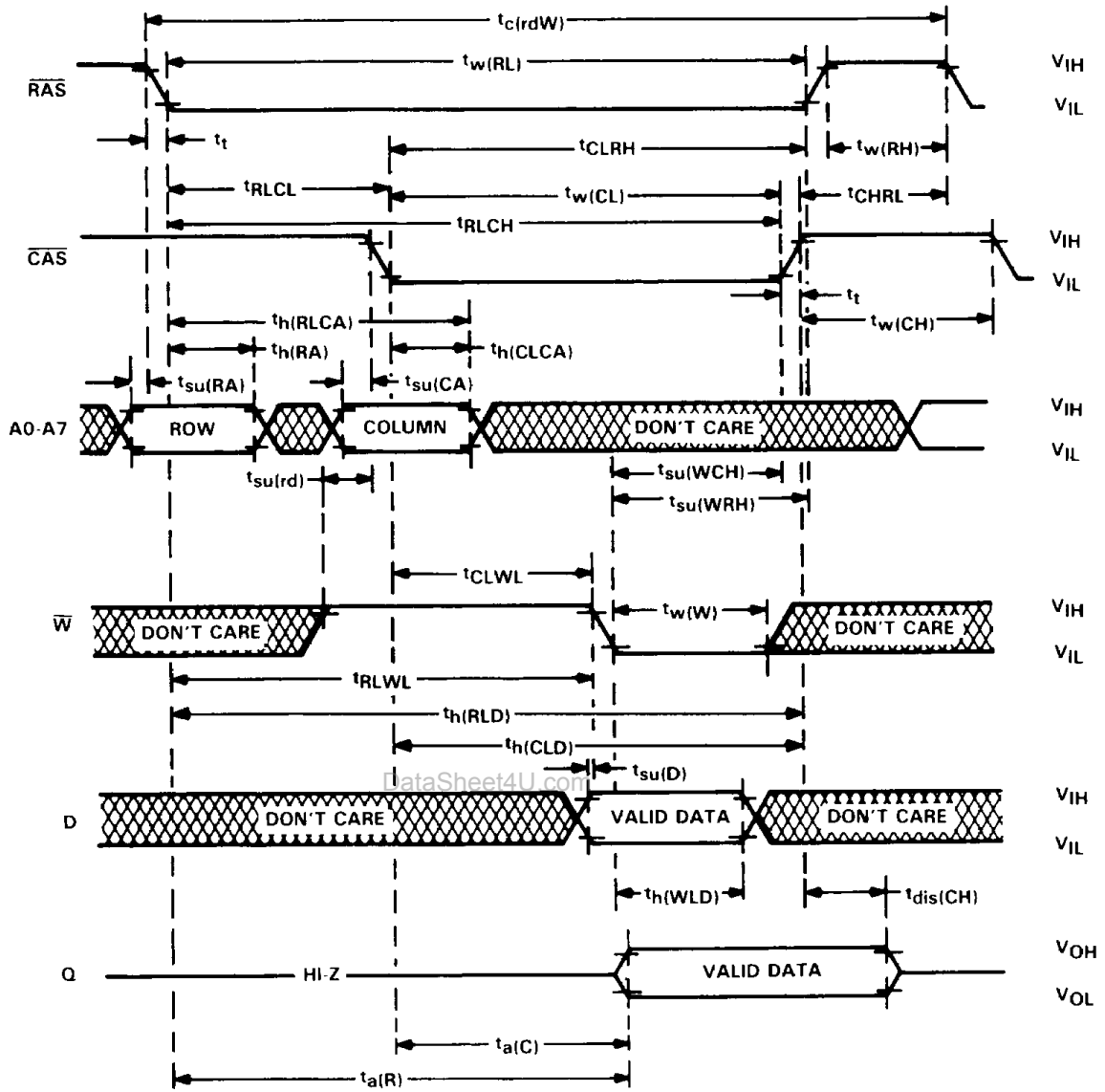
write cycle timing



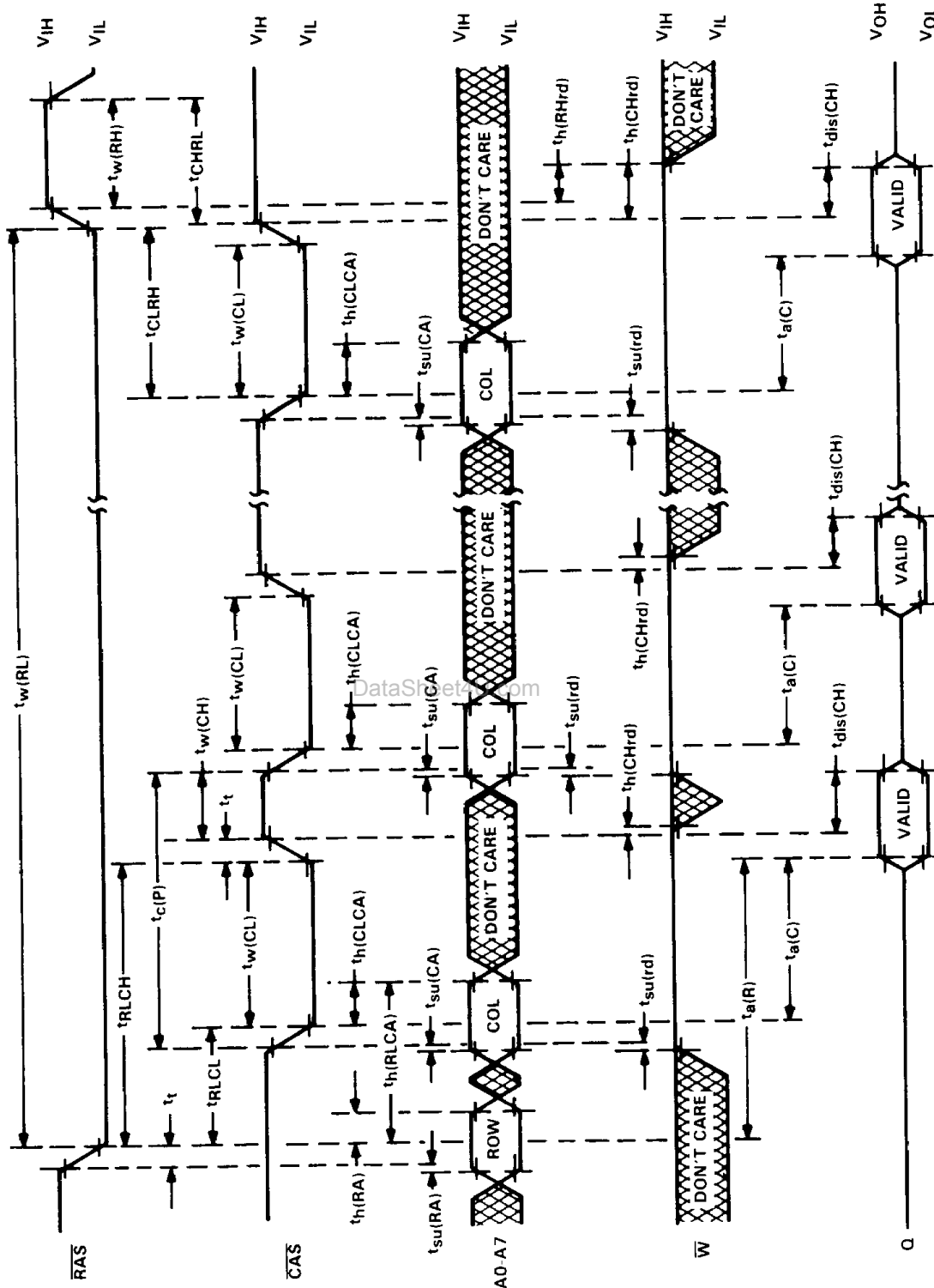
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

read-write/read-modify-write cycle timing



page-mode read cycle timing



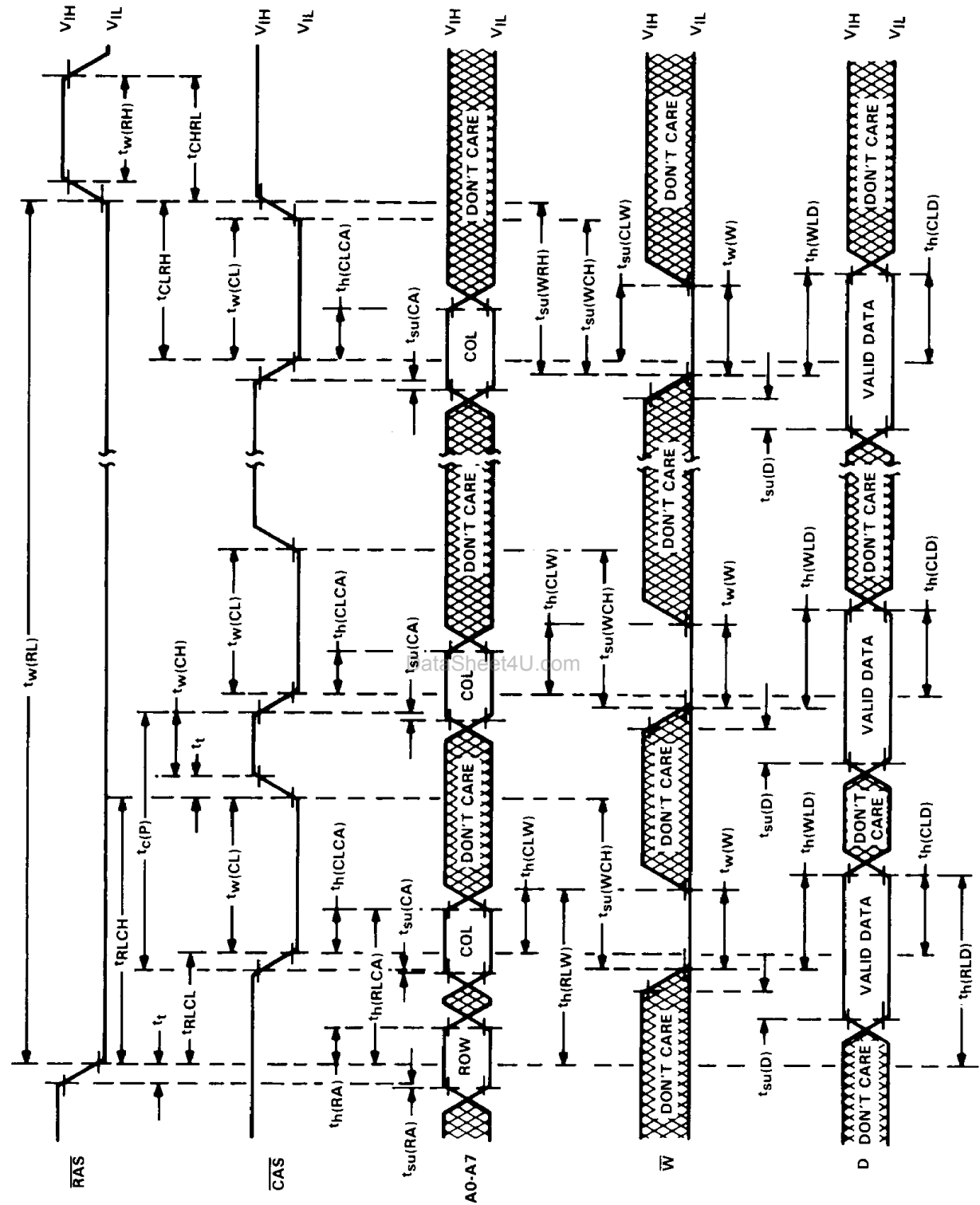
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.



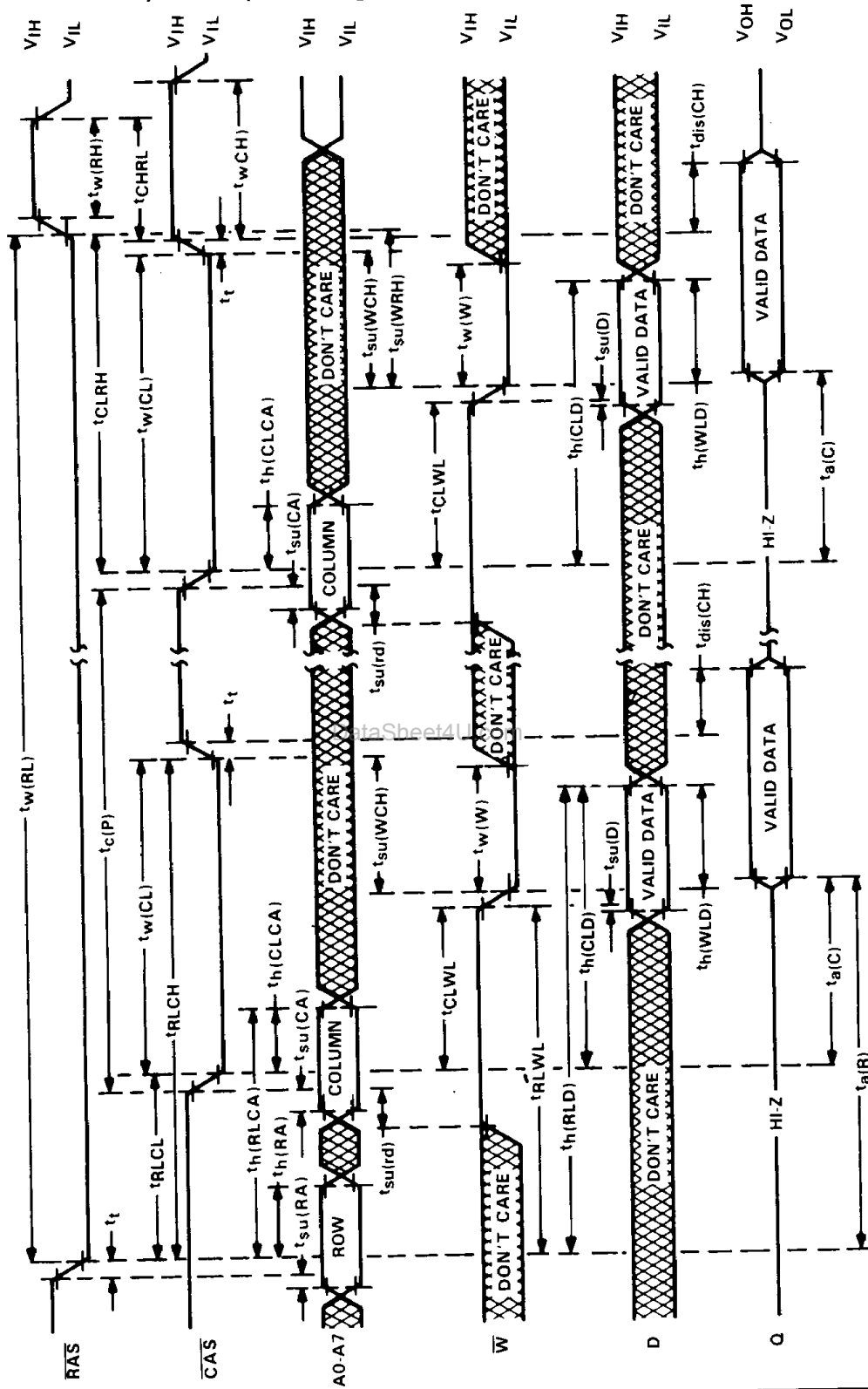
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

page-mode write cycle timing



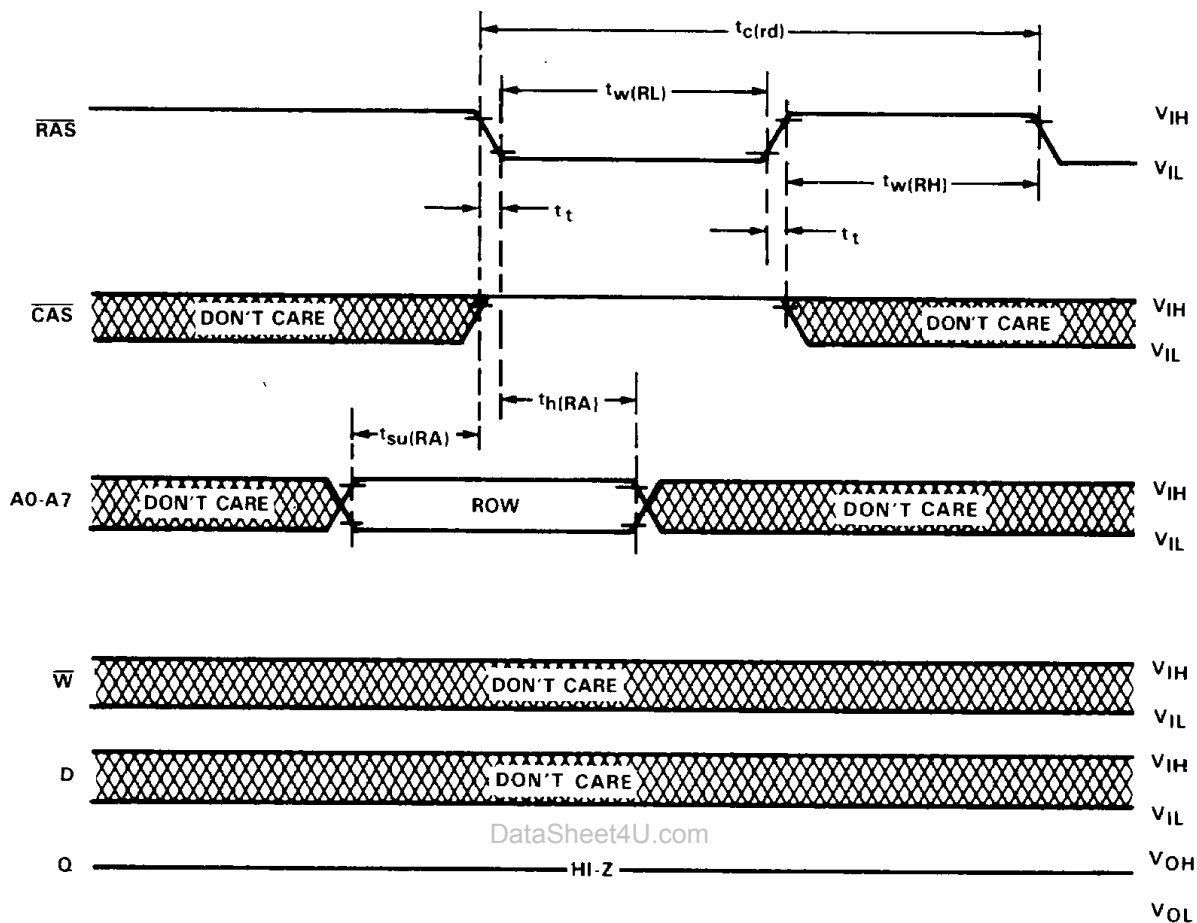
NOTE 6: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing


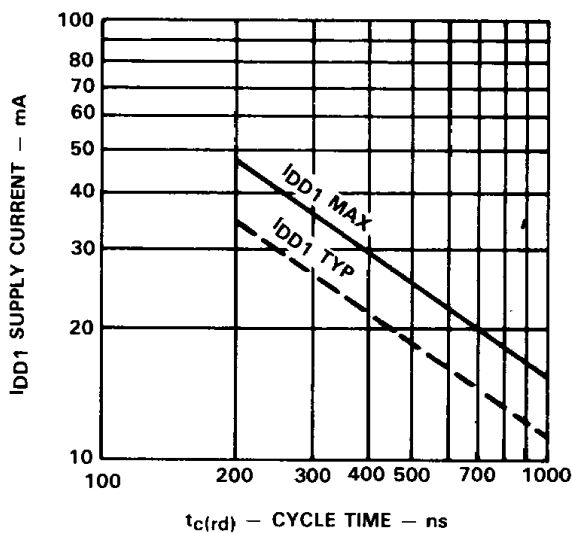
NOTE 7: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and the write timing specifications are not violated.

SMJ4164 65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

RAS-only refresh timing



IDD1 vs. CYCLE TIME



IDD3 vs. CYCLE TIME

