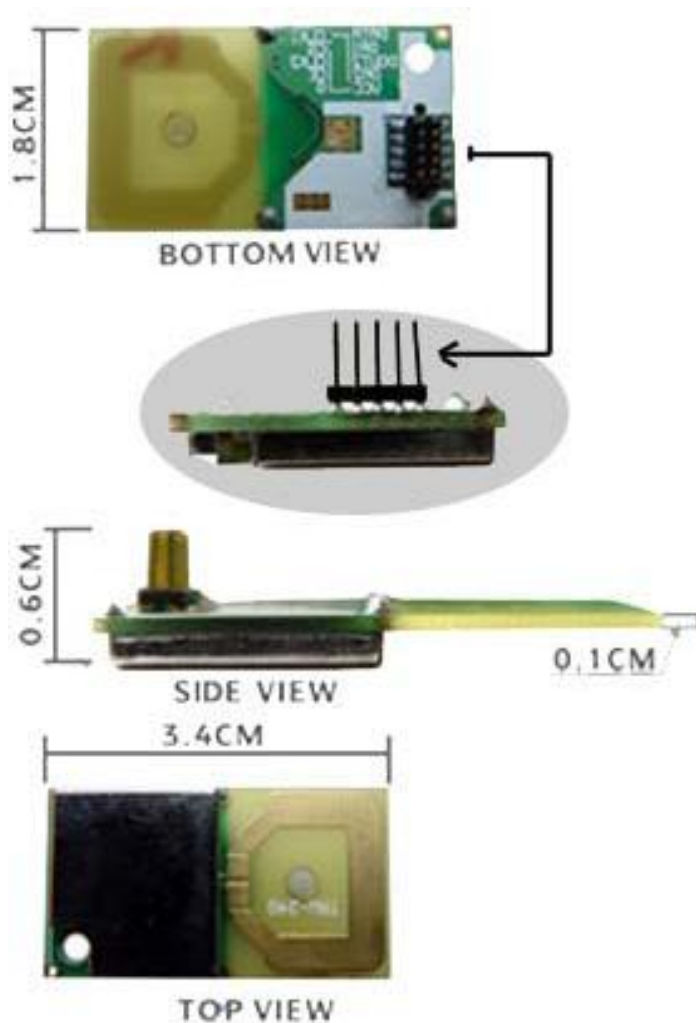


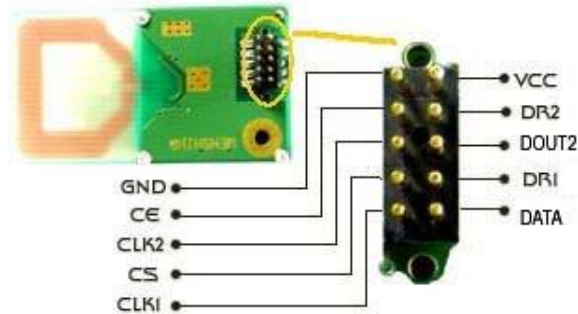
TRF-2.4G Reference Guide

Revision 1.01 –March 2004



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Pin Description



General Specifications

Conditions: VDD = +3V, VSS = 0V, T_A = -40°C to +85°C

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Operating conditions						
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	°C
Digital input pin						
V _{HI}	HIGH level input voltage		VDD-0.3		VDD	V
V _{LI}	LOW level input voltage		Vss		0.3	V
Digital output pin						
V _{OHI}	HIGH level output voltage (I _{OH} =-0.5mA)		VDD-0.3		VDD	V
V _{OL}	LOW level output voltage (I _{OL} =0.5mA)		Vss		0.3	V
General RF conditions						
f _{OP}	Operating frequency	1)	2400		2524	MHz
Δf	Frequency deviation			±156		kHz
R _{DATA}	Data rate ShockBurst™		>0		1000	kbps
F _{CHANNEL}	Channel spacing			1		MHz
Transmitter operation						
P _{RF}	Maximum Output Power	4)		0	+4	dBm
P _{RF} C	RF Power Control Range		16	20		dB
P _{RF} C _R	RF Power Control Range Resolution				±3	dB
P _{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P _{AC2}	2 nd Adjacent Channel Transmit Power 2MHz				-20	dBm
P _{AC3}	3 rd Adjacent Channel Transmit Power 3MHz				-40	dBm
I _{VDD}	Supply current @ 0dBm output power	5)		13		mA
I _{VDD}	Supply current @ -20dBm output power	5)		8.8		mA
I _{VDD}	Average Supply current @ -5dBm output power, ShockBurst™	6)		0.8		mA
I _{VDD}	Average Supply current in stand-by mode	7)		12		μA
I _{VDD}	Average Supply current in power down			1		μA
Receiver operation						
I _{VDD}	Supply current one channel 250kbps			18		mA
I _{VDD}	Supply current one channel 1000kbps			19		mA
I _{VDD}	Supply current two channels 250kbps			23		mA
I _{VDD}	Supply current two channels 1000kbps			25		mA
RX _{SENS}	Sensitivity at 0.1%BER (@250kbps)			-90		dBm
RX _{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-80		dBm
C/I _{CO}	C/I Co-channel			6		dB
C/I _{1ST}	1 st Adjacent Channel Selectivity C/I 1MHz			-1		dB
C/I _{2ND}	2 nd Adjacent Channel Selectivity C/I 2MHz			-16		dB
C/I _{3RD}	3 rd Adjacent Channel Selectivity C/I 3MHz			-26		dB
RX _B	Blocking Data Channel 2			-41		dB

ShockBurst™

The ShockBurst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling extremely power reduction.

When operating the **TRF-2.4G** in ShockBurst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.

By putting all high speed signal processing related to RF protocol on-chip, the **TRF-2.4G** offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly reduced risk of 'on-air' collisions due to short transmission time

The **TRF-2.4G** can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.

By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the nRF ShockBurst™ mode reduces the average current consumption in applications considerably.

ShockBurst™ principle

When the **TRF-2.4G** is configured in ShockBurst™, TX or RX operation is conducted in the following way (10 kbps for the example only).

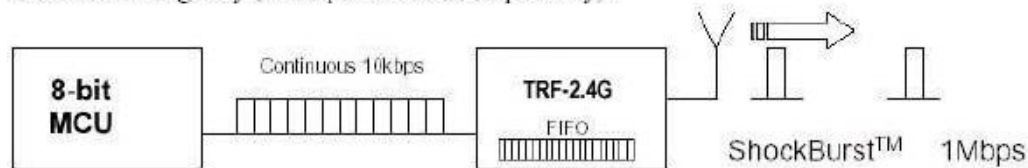


Figure 4 Clocking in data with MCU and sending with ShockBurst™ technology

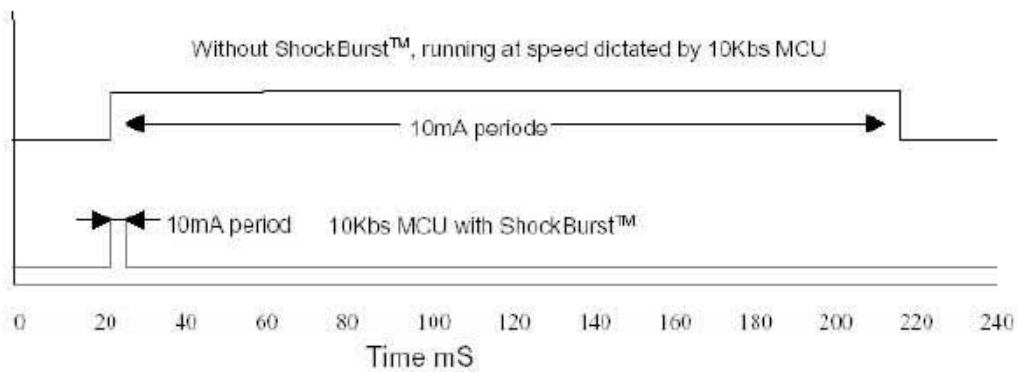


Figure 1 Current consumption with & without ShockBurst™ technology

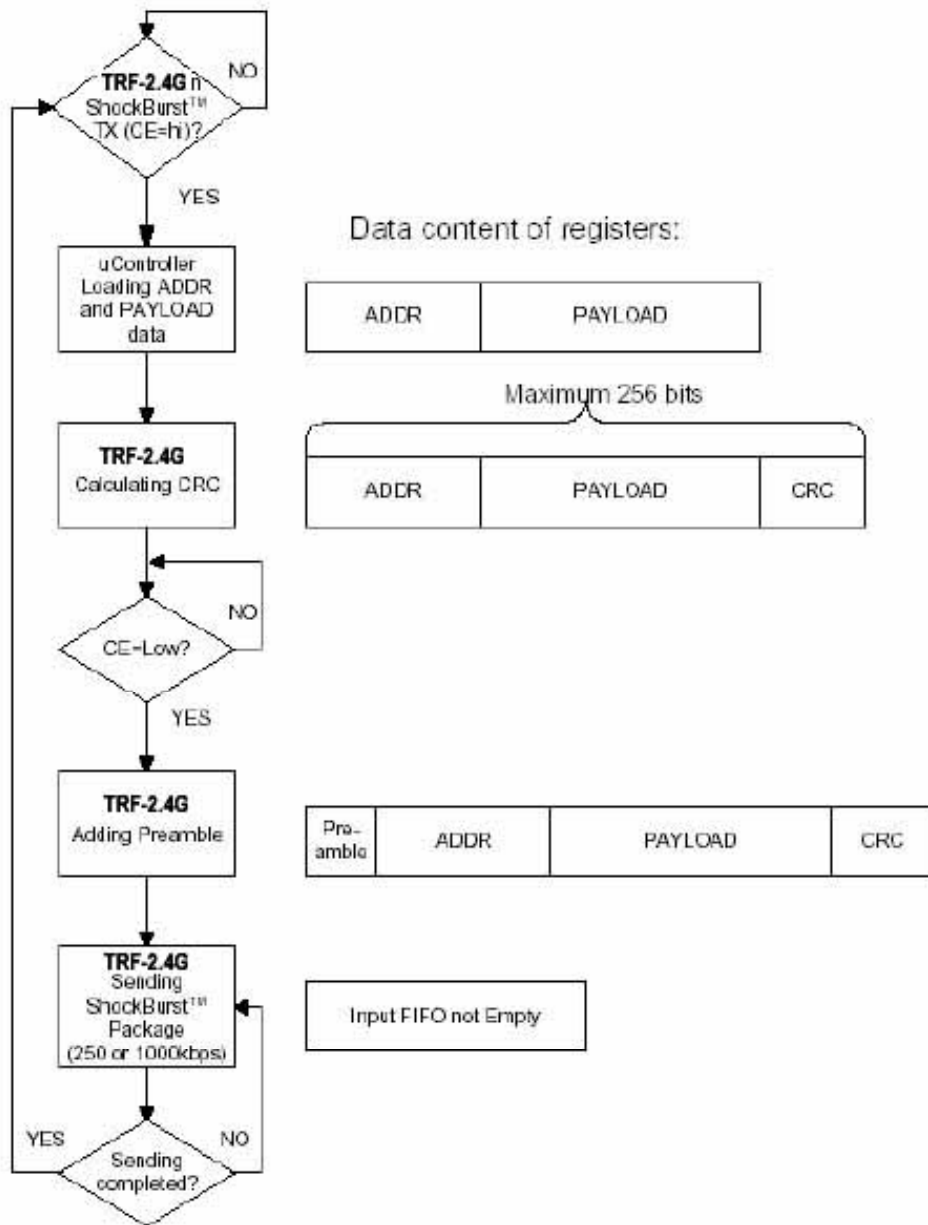


Figure 2 Flow Chart ShockBurst™ Transmit of TRF-2.4G

ShockBurst™ Transmit:

MCU interface pins: CE, CLK1, DATA

1. When the application MCU has data to send, set CE high. This activates **TRF-2.4G** on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the **TRF-2.4G**. The application protocol or MCU sets the speed <1Mbps (ex: 10kbps).
3. MCU sets CE low, this activates a **TRF-2.4G** ShockBurst™ transmission.
4. **TRW-2.4G** ShockBurst™:
 - RF front end is powered up
 - RF package is completed (preamble added, CRC calculated)
 - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
 - **TRF-2.4G** return to stand-by when finished

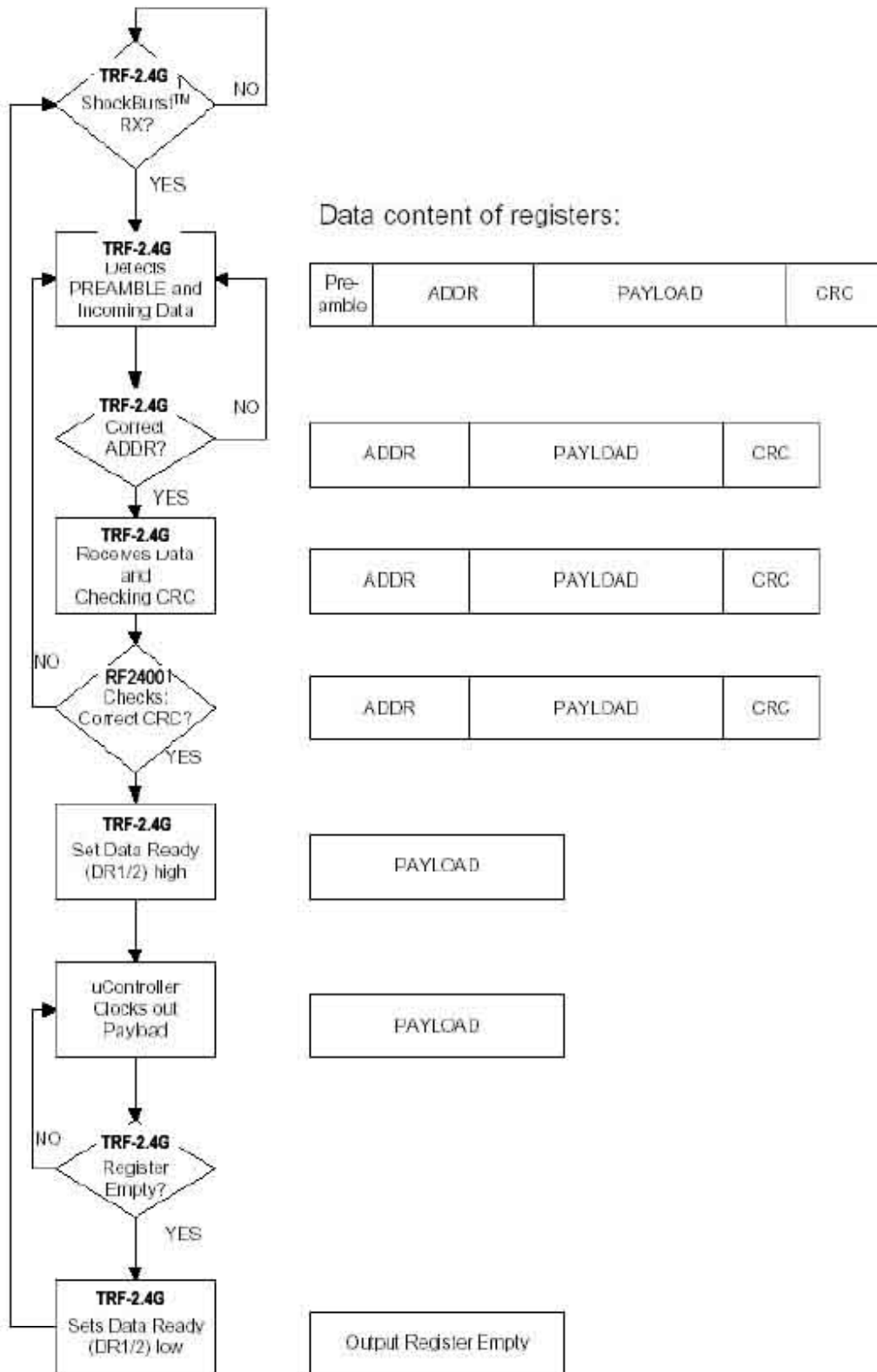


Figure 3 Flow Chart ShockBurst™ Receive of TRF-2.4G

RF2400DV ShockBurst™ Receive:

MCU interface pins: CE, DR1, CLK1 and DATA (one RX channel receive)

1. Correct address and size of payload of incoming RF packages are set when **TRF-2.4G** is configured to ShockBurst™ RX.
2. To activate RX, set CE high.
3. After 200 μ s settling, **TRF-2.4G** is monitoring the air for incoming communication.
4. When a valid package has been received (correct address and CRC found), **TRF-2.4G** removes the preamble, address and CRC bits.
5. **TRF-2.4G** then notifies (interrupts) the MCU by setting the DR1 pin high.
6. MCU may (or may not) set the CE low to disable the RF front end (low current mode).
7. The MCU will clock out just the payload data at a suitable rate (ex. 10 kbps).
8. When all payload data is retrieved **TRF-2.4G** sets DR1 low again, and is ready for new incoming data package if CE is kept high during data download. If the CE was set low, a new start up sequence can begin, see Figure 12.

DuoCeiver™ Simultaneous Two Channel Receive Mode

In both ShockBurst™ modes the TRF-24G can facilitate simultaneous reception of two parallel independent frequency channels at the maximum data rate. This means:

- TRF-24G can receive data from two 1 Mbps transmitters (ex: TRF-24G) 8 MHz (8 frequency channels) apart through one antenna interface.
- The output from the two data channels is fed to two separate MCU interfaces.
 - Data channel 1: CLK1, DATA, and DR1
 - Data channel 2: CLK2, DOUT2, and DR2
 - DR1 and DR2 are available only in ShockBurst™.

The TRF-24G DuoCeiver™ technology provides 2 separate dedicated data channels for RX and replaces the need for two, stand alone receiver systems.

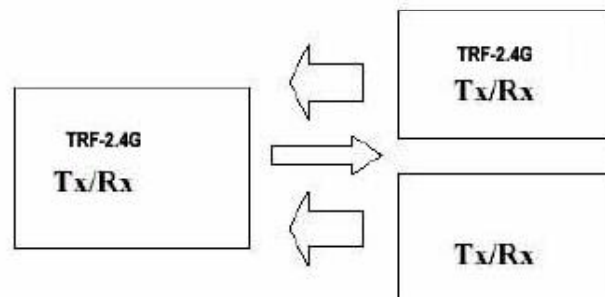


Figure 4 Simultaneous 2 channel receive on TRF-24G

There is one absolute requirement for using the second data channel. For the TRF-24G to be able to receive at the second data channel the frequency channel must be 8MHz higher than the frequency of data channel 1. The TRF-24G must be programmed to receive at the frequency of data channel 1. No time multiplexing is used in TRF-24G to fulfil this function. In direct mode the MCU must be able to handle two simultaneously incoming data packets if it is not multiplexing between the two data channels. In ShockBurst™ it is possible for the MCU to clock out one data channel at a time while data on the other data channel waits for MCU availability, without any lost data packets, and by doing so reduce the needed performance of the MCU.

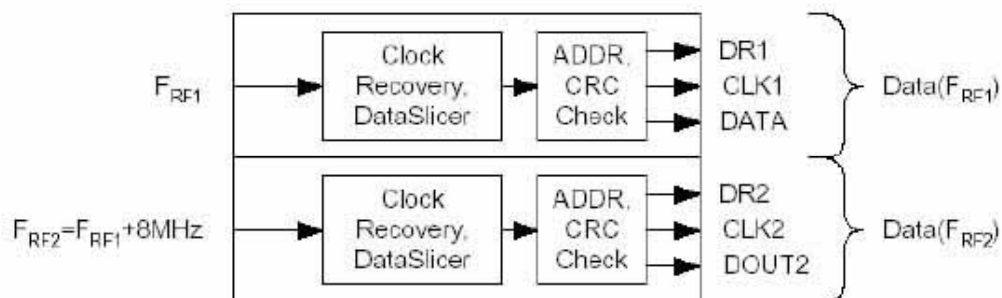


Figure 5 DuoCeiver™ with two simultaneously independent receive channels.

DEVICE CONFIGURATION

All configuration of the **TRF-2.4G** is done via a 3-wire interface to a single configuration register. The configuration word can be up to 15 bytes long for ShockBurst™

Configuration for ShockBurst™ operation

The configuration word in ShockBurst™ enables the **TRF-2.4G** to handle the RF protocol. Once the protocol is completed and loaded into **TRF-2.4G** only one byte, bit[7:0], needs to be updated during actual operation.

The configuration blocks dedicated to ShockBurst™ is as follows:

- Payload section width: Specifies the number of payload bits in a RF package. This enables the **TRF-2.4G** to distinguish between payload data and the CRC bytes in a received package.
- Address width: Sets the number of bits used for address in the RF package. This enables the **TRF-2.4G** to distinguish between address and payload data.
- Address (RX Channel 1 and 2): Destination address for received data.
- CRC: Enables **TRF-2.4G** on-chip CRC generation and de-coding.

NOTE:

These configuration blocks, with the exception of the CRC, are dedicated for the packages that a **TRF-2.4G** s to receive.

In TX mode, the MCU must generate an address and a payload section that fits the configuration of the **TRF-2.4G** that is to receive the data.

When using the **TRF-2.4G** on-chip CRC feature ensure that CRC is enabled and uses the same length for both the TX and RX devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC
-----------	---------	---------	-----

Figure 10 Data packet set-up

Configuration Word overview

	Bit position	Number of bits	Name	Function
ShockBurst™ configuration	143:120	24	TEST	Reserved for testing
	119:112	8	DATA2_W	Length of data payload section RX channel 2
	111:104	8	DATA1_W	Length of data payload section RX channel 1
	103:64	40	ADDR2	Up to 5 byte address for RX channel 2
	63:24	40	ADDR1	Up to 5 byte address for RX channel 1
	23:18	6	ADDR_W	Number of address bits (both RX channels).
	17	1	CRC_L	8 or 16 bit CRC
	16	1	CRC_EN	Enable on-chip CRC generation/checking.
General device configuration	15	1	RX2_EN	Enable two channel receive mode
	14	1	CM	Communication mode (Direct or ShockBurst™)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12:10	3	XO_F	Crystal frequency
	9:8	2	RF_PWR	RF output power
	7:1	7	RF_CH#	Frequency channel
	0	1	RXEN	RX or TX operation

Table 1 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS.

NOTE.

On the falling edge of CS, the **TRF-2.4G** updates the number of bits actually shifted in during the last configuration.

Ex:

If the **TRF-2.4G** is to be configured for 2 channel RX in ShockBurst™, a total of 120 bits must be shifted in during the first configuration after VDD is applied.

Once the wanted protocol, modus and RF channel are set, only one bit (RXEN) is shifted in to switch between RX and TX.

Configuration Word Detailed Description

The following describes the function of the 144 bits (bit 143 = MSB) that is used to configure the **TRF-2.4G**

General Device Configuration: bit[15:0]

ShockBurst™ Configuration: bit[119:0]

Test Configuration: bit[143:120]

MSB		TEST								
D143	D142	D141	D140	D139	D138	D137	D136			
Reserved for testing										
1	0	0	0	0	1	1	1	0	Default	

MSB		TEST															
D135	D134	D133	D132	D131	D130	D129	D128	D127	D126	D125	D124	D123	D122	D121	D120		
Reserved for testing															Close PLL on TX		
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	Default	

DATA2_W									
D119	D118	D117	D116	D115	D114	D113	D112		
Data width channel#2 in # of bits excluding addr/erc									
0	0	1	0	0	0	0	0	Default	

DATA1_W									
D111	D110	D109	D108	D107	D106	D105	D104		
Data width channel#1 in # of bits excluding addr/erc									
0	0	1	0	0	0	0	0	Default	

ADDR2													
D103	D102	D101	...	D71	D70	D69	D68	D67	D66	D65	D64		
Channel#2 Address RX (up to 40bit)													
0	0	0	...	1	1	1	0	0	1	1	1	Default	

ADDR1													
D63	D62	D61	...	D31	D30	D29	D28	D27	D26	D25	D24		
Channel#1 Address RX (up to 40bit)													
0	0	0	...	1	1	1	0	0	1	1	1	Default	

ADDR_W							
D23	D22	D21	D20	D19	D18		
Address width in # of bits (both channels)							
0	0	1	0	0	0	Default	

CRC					
D17		D16			
CRC Mode 1 = 16bit, 0 = 8bit				CRC 1 = enable, 0 = disable	
0		1		Default	

RF-Programming														LSB			
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
Two Ch.		BUF	OD	XC		RF Power		Channel selection							RXEN		
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	Default	

Table 2 Configuration data word

The MSB bit should be loaded first into the configuration register.

Default configuration word: h8E08.1C20.2000.0000.00E7.0000.0000.E721.0F04.

ShockBurst™ configuration:

The section B[119:16] contains the segments of the configuration register dedicated to ShockBurst™ operational protocol. After VDD is turned on ShockBurst™ configuration is done once and remains set whilst VDD is present. During operation only the first byte for frequency channel and RX/TX switching need to be changed.

PLL_CTRL

PLL_CTRL		
D121	D120	PLL
0	0	Open TX/Closed RX
0	1	Open TX/Open RX
1	0	Closed TX/Closed RX
1	1	Closed TX/Open RX

Table 10 PLL setting.

Bit 121-120:

PLL_CTRL: Controls the setting of the PLL for test purposes. With closed PLL in TX no deviation will be present.

DATAx_W

DATA2 W							
119	118	117	116	115	114	113	112

DATA1 W							
111	110	109	108	107	106	105	104

Table 4 Number of bits in payload.

Bit 119 – 112:

DATA2_W: Length of RF package payload section for receive-channel 2.

Bit 111 – 104:

DATA1_W: Length of RF package payload section for receive-channel 1.

NOTE:

The total number of bits in a ShockBurst™ RF package may not exceed 256! Maximum length of payload section is hence given by:

$$DATAx_W(bits) = 256 - ADDR_W - CRC$$

Where:

ADDR_W: length of RX address set in configuration word B[23:18]

CRC: check sum, 8 or 16 bits set in configuration word B[17]

PRE: preamble, 4 or 8 bits are automatically included

Shorter address and CRC leaves more room for payload data in each package.

ADDRx

ADDR2											
103	102	101	...	71	70	69	68	67	66	65	64
ADDR1											
63	62	61	...	31	30	29	28	27	26	25	24

Table 5 Address of receiver #2 and receiver #1.

Bit 103 – 64:

ADDR2: Receiver address channel 2, up to 40 bit.

Bit 63 – 24: ADDR1

ADDR1: Receiver address channel 1, up to 40 bit.

NOTE!

Bits in ADDR_x exceeding the address width set in ADDR_W are redundant and can be set to logic 0.

ADDR_W & CRC

ADDR_W						CRC_L	CRC_EN
23	22	21	20	19	18	17	16

Table 6 Number of bits reserved for RX address + CRC setting.

Bit 23 – 18:

ADDR_W: Number of bits reserved for RX address in ShockBurst™ packages.

NOTE:

Maximum number of address bits is 40 (5 bytes). Values over 40 in ADDR_W are not valid.

Bit 17:

CRC_L: CRC length to be calculated by **TRF-2.4G** in ShockBurst™.
 Logic 0: 8 bit CRC
 Logic 1: 16 bit CRC

Bit: 16:

CRC_EN: Enables on-chip CRC generation (TX) and verification (RX).
 Logic 0: On-chip CRC generation/checking disabled
 Logic 1: On-chip CRC generation/checking enabled

NOTE:

An 8 bit CRC will increase the number of payload bits possible in each ShockBurst™ data packet, but will also reduce the system integrity.

General device configuration:

This section of the configuration word handles RF and device related parameters.

Modes:

RX2_EN	CM	RFDR_SB	XO F			RF PWR	
15	14	13	12	11	10	9	8

Table 7 RF operational settings.

Bit 15:

RX2_EN:

Logic 0: One channel receive
Logic 1: Two channels receive

NOTE:

In two channels receive, the **TRF-2.4G** receives on two, separate frequency channels simultaneously. The frequency of receive channel 1 is set in the configuration word B[7-1], receive channel 2 is always 8 channels (8 MHz) above receive channel 1.

Bit 14:

Communication Mode:

Logic 1: **TRF-2.4G** operates in ShockBurst™ mode

Bit 13:

RF Data Rate:

Logic 0: 2. **TRF-2.4G**
Logic 1: 1 Mbps

NOTE:

Utilizing 250 kbps instead of 1Mbps will improve the receiver sensitivity by 10 dB. 1Mbps requires 16MHz crystal.

Bit 12-10:

D12	D11	D10
0	1	1

Table 8

Bit 9-8:

RF_PWR: Sets **TRF-24G** RF output power in transmit mode:

RF OUTPUT POWER		
D9	D8	P [dBm]
0	0	-20
0	1	-10
1	0	-5
1	1	0

Table 9 RF output power setting.

RF channel & direction

RF CH#							RXEN
7	6	5	4	3	2	1	0

Table 10 Frequency channel + RX / TX setting.

Bit 7 – 1:

RF_CH#: Sets the frequency channel the **TRF-24G** operates on.

The channel frequency in *transmit* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz}$$

RF_CH #: between 2400MHz and 2527MHz may be set.

The channel frequency in *data channel 1* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz} \text{ (Receive at PIN\#8)}$$

RF_CH #: between 2400MHz and 2524MHz may be set.

NOTE:

The channels above 83 can only be utilized in certain territories (ex: Japan)

The channel frequency in *data channel 2* is given by:

$$Channel_{RF} = 2400 \text{ MHz} + RF_CH\# \cdot 1.0 \text{ MHz} + 8\text{MHz} \text{ (Receive at PIN\#4)}$$

RF_CH #: between 2408MHz and 2524MHz may be set.

Bit 0:

Set active mode:

Logic 0: transmit mode

Logic 1: receive mode

DATA PACKAGE DESCRIPTION



Figure 7 Data Package Diagram

The data packet for both ShockBurst™ mode and direct mode communication is divided into 4 sections. These are:

1. PREAMBLE	<ul style="list-style-type: none"> · The preamble field is required in ShockBurst.
2. ADDRESS	<ul style="list-style-type: none"> · The address field is required in ShockBurst. mode. · 8 to 40 bits length. · Address automatically removed from received packet in ShockBurst.mode
3. PAYLOAD	<ul style="list-style-type: none"> · The data to be transmitted · In Shock-Burst mode payload size is 256 bits minus the following:(Address: 8 to 40 bits. + CRC 8 or 16 bits).
4. CRC	<ul style="list-style-type: none"> · 8 or 16 bits length · The CRC is stripped from the received output data.

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	1	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	0

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	1	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	1	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	0

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	1	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	1	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	1	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	0

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	0

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	0	0	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

Bit143	Bit142	Bit141	Bit140	Bit139	Bit138	Bit137	Bit136
1	0	0	0	1	1	1	0
Bit135	Bit134	Bit133	Bit132	Bit131	Bit130	Bit129	Bit128
0	0	0	0	1	0	0	0
Bit127	Bit126	Bit125	Bit124	Bit123	Bit122	Bit121	Bit120
0	0	0	1	1	1	0	0
Bit119	Bit118	Bit117	Bit116	Bit115	Bit114	Bit113	Bit112
1	1	0	0	1	0	0	0
Bit111	Bit110	Bit109	Bit108	Bit107	Bit106	Bit105	Bit104
1	1	0	0	1	0	0	0
Bit103	Bit102	Bit101	Bit100	Bit99	Bit98	Bit97	Bit96
1	1	0	0	0	0	0	0
Bit95	Bit94	Bit93	Bit92	Bit91	Bit90	Bit89	Bit88
1	0	1	0	1	0	1	0
Bit87	Bit86	Bit85	Bit84	Bit83	Bit82	Bit81	Bit80
0	1	0	1	0	1	0	1
Bit79	Bit78	Bit77	Bit76	Bit75	Bit74	Bit73	Bit72
1	0	1	0	1	0	1	0
Bit71	Bit70	Bit69	Bit68	Bit67	Bit66	Bit65	Bit64
0	1	0	1	0	1	0	1
Bit63	Bit62	Bit61	Bit60	Bit59	Bit58	Bit57	Bit56
1	0	1	0	1	0	1	0
Bit55	Bit54	Bit53	Bit52	Bit51	Bit50	Bit49	Bit48
0	1	0	1	0	1	0	1
Bit47	Bit46	Bit45	Bit44	Bit43	Bit42	Bit41	Bit40
1	0	1	0	1	0	1	0
Bit39	Bit38	Bit37	Bit36	Bit35	Bit34	Bit33	Bit32
0	1	0	1	0	1	0	1
Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
1	0	1	0	1	0	1	0
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
1	0	1	0	0	0	1	1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	0	1	0	1	1	1	1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	1	0	1	0	1

IMPORTANT TIMING DATA

The following timing applies for operation **TRF-2.4G**

TRF-2.4G Timing Information

TRF-2.4G timing	Max.	Min.	Name
VDD OFF → ST_BY mode	3ms		Tpd2sby
VDD OFF → Active mode (RX/TX)	3ms		Tpd2a
ST_BY → TX ShockBurst™	195µs		Tsby2txSB
ST_BY → TX Direct Mode	202µs		Tsby2txDM
ST_BY → RX mode	202µs		Tsby2rx
Minimum delay from CS to data.		5µs	Tcs2data
Minimum delay from CE to data.		5µs	Tce2data
Minimum delay from DR1/2 to clk.		50ns	Tdr2clk
Maximum delay from clk to data.	50ns		Tclk2data
Delay between edges		50ns	Td
Setup time		500ns	Ts
Hold time		500ns	Th
Delay to finish internal GFSK data		1/data rate	Tfd
Minimum input clock high		500ns	Thmin
Set-up of data in Direct Mode	50ns		Tsdm
Minimum clock high in Direct Mode		300ns	Thdm
Minimum clock low in Direct Mode		230ns	Tldm

Table 11 Switching times

When **TRF-2.4G** is in power down it must always settle in stand-by (Tpd2sby) before it can enter configuration or one of the active modes.

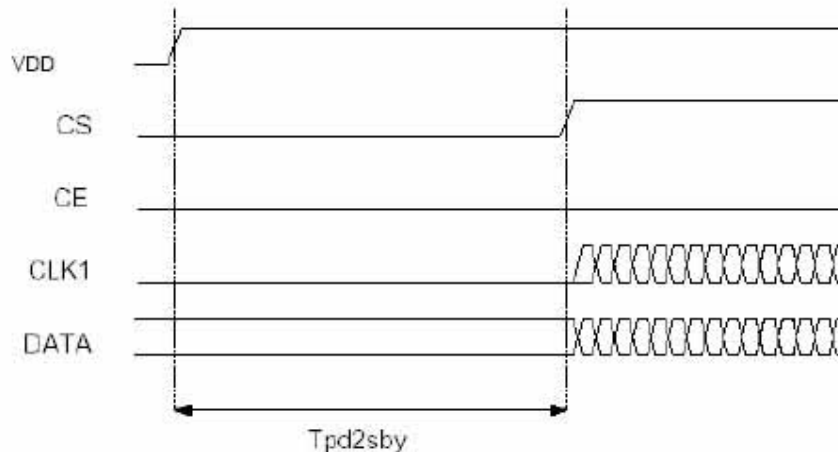


Figure 8 Timing diagram for **TRF-2.4G** (or VDD off) to stand by mode

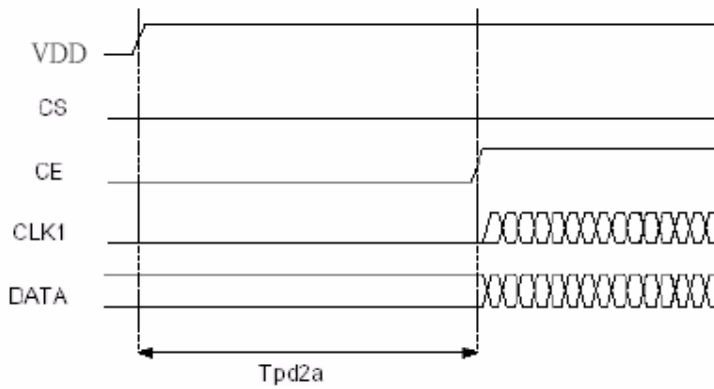


Figure 9 VDD off to active mode

Note that the configuration word will be lost when VDD is turned off and that the device then must be configured before going to one of the active modes. If the device is configured one can go directly from power down to the wanted active mode.

Note:

CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.

Configuration mode timing

When one or more of the bits in the configuration word needs to be changed the following timing apply.

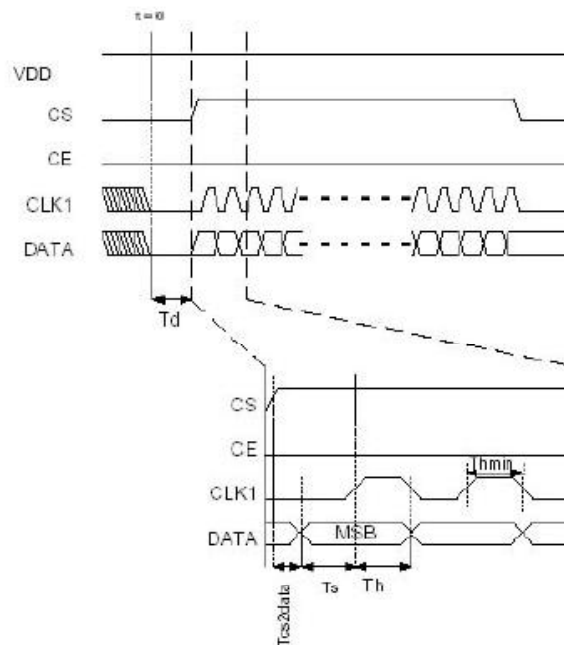


Figure 10 Timing diagram for configuration

If configuration mode is entered from power down, CS can be set high after Tpd2sby as shown in Figure 8

ShockBurst™ Mode timing

ShockBurst™ TX:

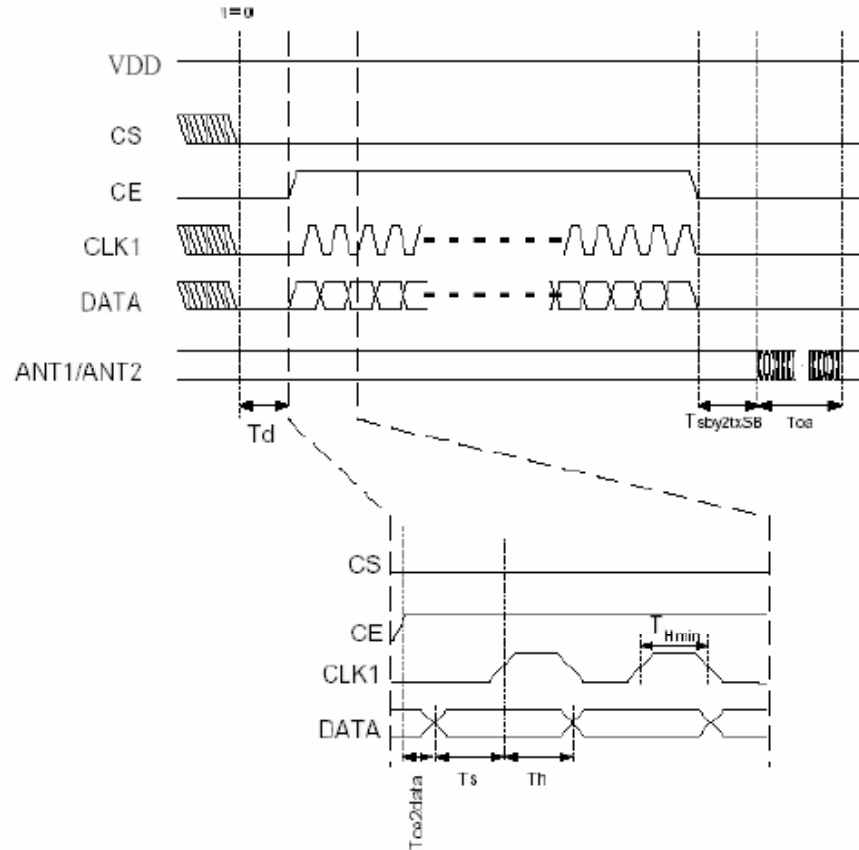


Figure 11 Timing of ShockBurst™ in TX

The package length and the data rate give the delay T_{oa} (time on air), as shown in the equation.

$$T_{oa} = 1 / \text{datarate} \cdot (\# \text{ databits} + 1)$$

ShockBurst™ RX:

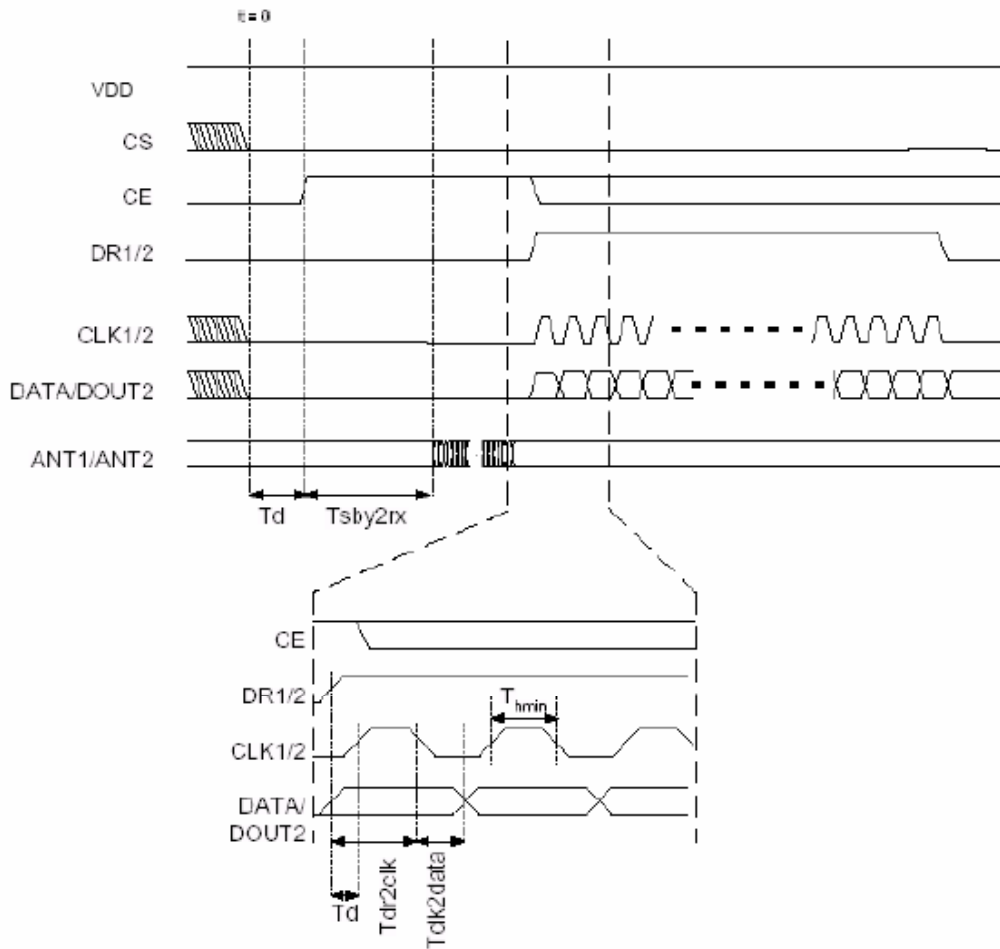


Figure 12 Timing of ShockBurst™ in RX

The CE may be kept high during downloading of data, but the cost is higher current consumption (18mA) and the benefit is no start-up time (200µs) after the DR1 goes low.

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	13.0 mA
10	-5 dBm ±3dB	10.5 mA
01	-10 dBm ±3dB	9.4 mA
00	-20 dBm ±3dB	8.8 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = 400 Ω.

```

=====
===== 2.4G test program =====
===== MCU: EM78P156E =====
===== MCU CRYSTALL:6MHZ =====
===== RF CRYSTALL:20MHZ =====
=====

```

```

          _____
PW  --|P52      P51|-- T_LED1
      --|P53      P50|-- R_LED2
      --|TCC      OSCI|--
      --|/RST     OSCO|--
      --|VSS      VCC|--
KEY_1 --|P60      P67|-- CS
KEY_2 --|P61      P66|-- DR1
      --|P62      P65|-- CLK1
CE  --|P63      P64|-- DATA
          |_____
          EM78P156E

```

```

-----
ICC      EQU  0X1
P5       EQU  0X5
P6       EQU  0X6
FLAG     EQU  0X1F
BYTE     EQU  0X1E
R0       EQU  0X1D
DLY_REG  EQU  0X1C
KEY_REG  EQU  0X1B
TIMER_REG EQU  0X1A
-----

```

```

ORG      0X0
JMP      RESET
JMP      INT_0

```

```
ORG 0X8
JMP INT_1
```

RF_CONFIG_TABLE:

```
MOV A,R0
ADD 0X2,A

RETL 0X8E ;TEST
RETL 0X08
RETL 0X1C

RETL 0X20 ;DATA2_W

RETL 0X0D0 ;DATA1_W

RETL 0X0BB ;ADDR2
RETL 0X0BB
RETL 0X0BB
RETL 0X0BB
RETL 0X0BB

RETL 0X12 ;ADDR1
RETL 0X34
RETL 0X56
RETL 0X78
RETL 0X9A

RETL 0X0A1 ;ADDR_W/CRC

RETL 0X53 ;RF-PROGRAMMING
RETL 0X02
```

```
-----
ADDRESS_TABLE: MOV A,R0
ADD 0X2,A
RETL 0X12 ;ADDR1
RETL 0X34
RETL 0X56
```

```

RETL  0X78
RETL  0X9A

;-----
RESET:
MOV   A,@0X0
IOW  0XF
IOW  0XE
MOV   A,@0X0FF
IOW  0XB
MOV   A,@0X0F8
IOW  0XD

MOV   A,@0X08      ;P5,0-LED P5,1-LED P5,2-PW
P5,3-CRYSTALL_SELECT
IOW  0X5
MOV   A,@0X47      ;P6,0-KEY P6,1-KEY P6,2-KEY
P6,3-CE
IOW  0X6           ;P6,4-DATA P6,5-CLK1 P6,6-DR1 P6,7-CS
BC   P6,3      ;CE
BC   P6,7      ;CS
MOV   A,@0X0D      ;WDT
CONTW
MOV   A,@0X80
IOW  0XE      ;WATCHDOG ENABLE

MOV   A,@0X2F
MOV   0X3F,A
MOV   A,@0X10
MOV   0X4,A
CLEAR_REG: CLR0X0
INC   0X4
DJZ   0X3F
JMP   CLEAR_REG

MOV   A,@0X3
MOV   0X10,A

```

```

S_LED_TEST:
    MOV    A,@0X0FF
    MOV    0X11,A
S_LED_TEST1:
    CALL   DELAY1MS
    CALL   DELAY1MS
    WDTC
    JBS    0X11,7
    JMP    S_LED_OFF
    BS     P5,0    ;LED
    BS     P5,1    ;LED
    JMP    S_SKIP
S_LED_OFF:
    BC     P5,0    ;LED
    BC     P5,1    ;LED
S_SKIP:
    DJZ    0X11
    JMP    S_LED_TEST1
    DJZ    0X10
    JMP    S_LED_TEST
;
;
;===== MAIN PROGRAM =====
;
MAIN_LOOP:
    BS     P5,2    ;PW
    BC     P5,0    ;R_LED
    BC     P5,1    ;T_LED
    BC     P6,3    ;CE

    CALL   DELAY1MS
    MOV    A,P6
    AND    A,@0X07
    MOV    KEY_REG,A
    JBC    P5,3    ;CRYSTALL SELECT<0-16M 1-20M>
    BS     KEY_REG,3

    MOV    A,KEY_REG

```

```
AND  A,@0X03
XOR  A,@0X0
JBC  0X3,2    ;Z
JMP  T_MODEL
```

```
MOV  A,KEY_REG
AND  A,@0X03
XOR  A,@0X1
JBC  0X3,2    ;Z
JMP  R_MODEL
```

```
MOV  A,KEY_REG
AND  A,@0X03
XOR  A,@0X03
JBC  0X3,2    ;Z
JMP  SLEEP_MODEL
```

```
JMP  MAIN_LOOP
```

```
=====
T_MODEL:
```

```
BC   P5,0    ;R_LED
BC   P5,1    ;T_LED
CALL DATA_PRO
MOV  A,@0X1C    ;TX_ON  RX_OFF
MOV  0X22,A
MOV  A,@0X4F    ;250K 0db
JBC  P6,2    ;<0-250K  1-1000K>
MOV  A,@0X6F
```

```
MOV  0X30,A
MOV  A,@0X14    ;2410
MOV  0X31,A
CALL RF_CONFIG
CALL DELAY200US
CALL RF_CONFIG
CALL DELAY200US
```

```
T_LOOP:
```

```
BS    P5,1    ;T_LED
CALL  RF_SEND
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
CALL  DELAY1MS
WDTC
MOV   A,P6
AND   A,@0X07
MOV   BYTE,A
JBC   P5,3    ;KEY
BS    BYTE,3
MOV   A,BYTE
XOR   A,KEY_REG
JBC   0X3,2    ;Z
JMP   T_LOOP
BC    P5,1    ;T_LED
JMP   MAIN_LOOP
```

R_MODEL:

```
BC    P5,0    ;R_LED
BC    P5,1    ;T_LED
CALL  DATA_PRO
MOV   A,@0X1F    ;TX_OFF  RX_ON
MOV   0X22,A
MOV   A,@0X4F    ;250K 0db
JBC   P6,2    ;<0-250K  1-1000K>
MOV   A,@0X6F
MOV   0X30,A
MOV   A,@0X15    ;2410
MOV   0X31,A
CALL  RF_CONFIG
```

```
MOV A,@0X10
MOV 0X13,A
BS P6,3 ;CE
CLR TCC
BC 0XF,0 ;TIMER FLAG
MOV A,@0X1
IOW 0XF ;TIMER INTERRUPT ENABLE
R_SP1:
BC P5,0 ;R_LED
R_LOOP1:
MOV A,@0X060
MOV TIMER_REG,A
BC FLAG,0 ;INTERRUPT FLAG
DJZ 0X13
JMP R_LOOP
JMP R_MODEL

R_LOOP:
WDTC
JBC FLAG,0 ;INTERRUPT FLAG
JMP R_SP1
MOV A,P6
AND A,@0X7
MOV BYTE,A
JBC P5,3 ;KEY
BS BYTE,3
MOV A,BYTE
XOR A,KEY_REG
JBS 0X3,2 ;Z
JMP R_RET
JBS P6,6 ;DR1
JMP R_LOOP
BS P5,0 ;R_LED
MOV A,@0X10
MOV 0X13,A
CALL RF_RECEIVE
CALL DELAY1MS
```

```
        JMP     R_LOOP1

R_RET:
        BC     P6,3    ;CE
        BC     P5,0
        MOV    A,@0X0
        IOW   0XF
        JMP    MAIN_LOOP

;=====
SLEEP_MODEL:
        CALL   DATA_PRO
        BC     P5,0    ;R_LED
        BC     P5,1    ;T_LED
        CALL   DATA_PRO
        MOV    A,@0X1E    ;TX_OFF  RX_OFF
        MOV    0X22,A
        MOV    A,@0X4C    ;250K 0db
        JBC   P6,2    ;<0-250K  1-1000K>
        MOV    A,@0X6C
        MOV    0X30,A
        MOV    A,@0X15    ;2410
        MOV    0X31,A
        CALL   RF_CONFIG
        BC     P5,2    ;PW

S_LOOP:
        CALL   DELAY1MS
        WDTC
        MOV    A,P6
        AND   A,@0X07
        MOV    BYTE,A
        JBC   P5,3    ;KEY
        BS    BYTE,3
        MOV    A,BYTE
        XOR   A,KEY_REG
        JBC   0X3,2    ;Z
        JMP    S_LOOP
```

```
JMP    MAIN_LOOP

;=====
DATA_PRO:
    MOV    A,@0X20
    MOV    0X4,A
    CLR    R0
    MOV    A,@0X12    ;18
    MOV    0X10,A
DATA_LOOP:
    CALL   RF_CONFIG_TABLE
    MOV    0X0,A
    INC    R0
    INC    0X4
    DJZ    0X10
    JMP    DATA_LOOP
    RET

;=====
;==== RF CONFIG SUBROUTINE =====
;=====
RF_CONFIG:
    BC     P6,3    ;CE
    BS     P6,7    ;CS
    CALL   DELAY200US
    MOV    A,@0X12    ;18
    MOV    0X10,A
    MOV    A,@0X20
    MOV    0X4,A
RF_CONF_BYTE_LP:
    MOV    A,@0X8
    MOV    0X11,A
    MOV    A,0X0
    MOV    BYTE,A
RF_CONF_BIT_LP:
    BC     P6,5    ;CLK1
    JBS    BYTE,7
    BC     P6,4    ;DATA
    JBC    BYTE,7
```

```

    BS    P6,4    ;DATA
    RLC   BYTE
    BS    P6,5    ;CLK1
    DJZ   0X11
    JMP   RF_CONF_BIT_LP
    INC   0X4
    DJZ   0X10
    JMP   RF_CONF_BYTE_LP
    CALL  DELAY5US
    BC    P6,5    ;CLK1
    BC    P6,7    ;CS
    RET

;=====
;===== RF SEND SUBROUTINE =====
;=====

RF_SEND:
    BC    P6,7    ;CS
    BS    P6,3    ;CE
    CALL  DELAY5US
    CALL  DELAY5US
    CLR   R0
    MOV   A,@0X5    ;ADDRESS BIT 5*8=40 BIT
    MOV   0X10,A

RF_S_ADD_BYTE:
    CALL  ADDRESS_TABLE
    MOV   BYTE,A
    MOV   A,@0X8
    MOV   0X11,A

RF_S_ADD_BIT:
    BC    P6,5    ;CLK1
    JBS   BYTE,7
    BC    P6,4    ;DATA
    JBC   BYTE,7
    BS    P6,4    ;DATA
    RLC   BYTE
    BS    P6,5    ;CLK1
    DJZ   0X11
    JMP   RF_S_ADD_BIT

```

```

    INC    R0
    DJZ    0X10
    JMP    RF_S_ADD_BYTE

    MOV    A,@0X1A      ;208 BIT DATA
    MOV    0X10,A
RF_S_D_BYTE:
    MOV    A,@0X8
    MOV    0X11,A
    MOV    A,@0X037
    MOV    BYTE,A
RF_S_D_BIT:
    BC    P6,5      ;CLK1
    JBS    BYTE,7
    BC    P6,4      ;DATA
    JBC    BYTE,7
    BS    P6,4      ;DATA
    RLC    BYTE
    BS    P6,5      ;CLK1
    DJZ    0X11
    JMP    RF_S_D_BIT
    DJZ    0X10
    JMP    RF_S_D_BYTE
    CALL   DELAY5US
    BC    P6,5      ;CLK1
    BC    P6,3      ;CE
    RET

=====
===== RF RECEIVE SUBROUTINE =====
=====
RF_RECEIVE:
    BC    P6,7      ;CS
    BC    P6,3      ;CE
    CALL   DELAY5US
    CALL   DELAY5US
    MOV    A,@0X20
    MOV    0X4,A
    MOV    A,@0X1A      ;208 bit

```

```

        INC    R0
        DJZ    0X10
        JMP    RF_S_ADD_BYTE

        MOV    A,@0X1A      ;208 BIT DATA
        MOV    0X10,A
RF_S_D_BYTE:
        MOV    A,@0X8
        MOV    0X11,A
        MOV    A,@0X037
        MOV    BYTE,A
RF_S_D_BIT:
        BC    P6,5      ;CLK1
        JBS    BYTE,7
        BC    P6,4      ;DATA
        JBC    BYTE,7
        BS    P6,4      ;DATA
        RLC    BYTE
        BS    P6,5      ;CLK1
        DJZ    0X11
        JMP    RF_S_D_BIT
        DJZ    0X10
        JMP    RF_S_D_BYTE
        CALL   DELAY5US
        BC    P6,5      ;CLK1
        BC    P6,3      ;CE
        RET

;=====
;===== RF RECEIVE SUBROUTINE =====
;=====

RF_RECEIVE:
        BC    P6,7      ;CS
        BC    P6,3      ;CE
        CALL   DELAY5US
        CALL   DELAY5US
        MOV    A,@0X20
        MOV    0X4,A
        MOV    A,@0X1A      ;208 bit

```

```
DLY_LOOP:
    NOP
    NOP
    NOP
    DJZ    DLY_REG
    JMP    DLY_LOOP
    RET

;=====
;===== INTERRUPT SUBROUTINE =====
;=====

INT_0:
INT_1:
    BC    0XF,0    ;TIMER FLAG
    DJZ    TIMER_REG
    JMP    INT_RET
    BS    FLAG,0    ;INTERRUPT FLAG
INT_RET:
    RETI
```