TL082
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (Bi-FET™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features
- Internally trimmed offset voltage: 15 mV
- Low input bias current: 50 pA
- Low input noise voltage: 16 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 3.6 mA
- High input impedance: 10^12 Ω
- Low total harmonic distortion \( A_v \mid_{V_o = 10, R_l = 10k, V_o = 20 Vp - p} < 0.02\%

Typical Connection

Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ±18V
Power Dissipation (Note 2) Operating Temperature Range 0˚C to +70˚C
Tj(MAX) 150˚C
Differential Input Voltage ±30V

Input Voltage Range (Note 3) ±15V
Output Short Circuit Duration Continuous
Storage Temperature Range −65˚C to +150˚C
Lead Temp. (Soldering, 10 seconds) 260˚C
ESD rating to be determined.

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

DC Electrical Characteristics (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TL082C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>Rs = 10 kΩ, TA = 25˚C Over Temperature</td>
<td>5</td>
<td>15 mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td>ΔVOS/ΔT</td>
<td>Average TC of Input Offset Voltage</td>
<td>Rs = 10 kΩ</td>
<td>10</td>
<td>μV/˚C</td>
</tr>
<tr>
<td>IOS</td>
<td>Input Offset Current</td>
<td>TJ = 25˚C, (Notes 5, 6) TJ ≤ 70˚C</td>
<td>25</td>
<td>200 pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>nA</td>
</tr>
<tr>
<td>IB</td>
<td>Input Bias Current</td>
<td>TJ = 25˚C, (Notes 5, 6) TJ ≤ 70˚C</td>
<td>50</td>
<td>400 pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>nA</td>
</tr>
<tr>
<td>RIN</td>
<td>Input Resistance</td>
<td>TJ = 25˚C</td>
<td>1012</td>
<td>Ω</td>
</tr>
<tr>
<td>AVOL</td>
<td>Large Signal Voltage Gain</td>
<td>VS = ±15V, TA = 25˚C</td>
<td>25</td>
<td>100 V/mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VOS = ±10V, RL = 2kΩ Over Temperature</td>
<td>15</td>
<td>V/mV</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage Swing</td>
<td>VS = ±15V, RL = 10 kΩ Over Temperature</td>
<td>±12</td>
<td>±13.5 V</td>
</tr>
<tr>
<td>VCM</td>
<td>Input Common-Mode Voltage Range</td>
<td>VS = ±15V</td>
<td>±11</td>
<td>±15 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>−12</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>Rs ≤ 10 kΩ</td>
<td>70</td>
<td>100 dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td>(Note 7)</td>
<td>70</td>
<td>100 dB</td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current</td>
<td></td>
<td>3.6</td>
<td>5.6 mA</td>
</tr>
</tbody>
</table>

AC Electrical Characteristics (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>TL082C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Amplifier to Amplifier Coupling</td>
<td>TA = 25˚C, f = 1Hz-20 kHz (Input Referred)</td>
<td>−120</td>
<td>dB</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>VS = ±15V, TA = 25˚C</td>
<td>8</td>
<td>13 V/μs</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth Product</td>
<td>VS = ±15V, TA = 25˚C</td>
<td>4</td>
<td>MHz</td>
</tr>
<tr>
<td>ei</td>
<td>Equivalent Input Noise Voltage</td>
<td>TA = 25˚C, RB = 100kΩ, f = 1000 Hz</td>
<td>25</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.01</td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

Note 2: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115˚C/W junction to ambient for the N package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for VS = ±15V and 0˚C ≤ TA ≤ 70˚C. VOS, IB, and IOS are measured at VCM = 0.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, TJ. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation. PD = θJA TJ + θJA PD where θJA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

V5 = ±6V to ±15V.
Typical Performance Characteristics

- **Input Bias Current**
- **Supply Current**
- **Positive Common-Mode Input Voltage Limit**
- **Negative Common-Mode Input Voltage Limit**
- **Positive Current Limit**
- **Voltage Swing**
- **Output Voltage Swing**
Typical Performance Characteristics (Continued)

**Gain Bandwidth**

Gain Bandwidth vs Temperature

**Bode Plot**

Bode Plot showing Gain and Phase vs Frequency

**Slew Rate**

Slew Rate vs Temperature

**Distortion vs Frequency**

Distortion vs Frequency

**Undistorted Output Voltage Swing**

Undistorted Output Voltage Swing vs Frequency

**Open Loop Frequency Response**

Open Loop Frequency Response vs Frequency

**Common-Mode Rejection Ratio**

Common-Mode Rejection Ratio vs Frequency

**Power Supply Rejection Ratio**

Power Supply Rejection Ratio vs Frequency

**Equivalent Input Noise Voltage**

Equivalent Input Noise Voltage vs Frequency

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Typical Performance Characteristics (Continued)

Pulse Response

Small Signal Inverting

Output Impedance

Large Signal Inverting

Inverter Setting Time

Large Signal Non-Inverting

Small Signal Non-Inverting

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Pulse Response (Continued)

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (Bi-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling. As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.
Detailed Schematic

Three-Band Active Tone Control

Typical Applications
Typical Applications (Continued)

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Note 8: All controls flat.
Note 9: Bass and treble boost, mid flat.
Note 10: Bass and treble cut, mid flat.
Note 11: Mid boost, bass and treble flat.
Note 12: Mid cut, bass and treble flat.

Improved CMRR Instrumentation Amplifier

\[ A_v = \left( \frac{2R_2}{R_1} + 1 \right) \frac{R_5}{R_4} \]

\( \# \) and \( \# \) are separate isolated grounds
Matching of R2’s, R4’s and R5’s control CMRR
With \( A_v = 1400 \), resistor matching = 0.01%: CMRR = 136 dB
- Very high input impedance
- Super high CMRR

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Typical Applications (Continued)

Fourth Order Low Pass Butterworth Filter

- Corner frequency \( f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \)
- Passband gain \( H_p = (1 + \frac{R_4}{R_3}) (1 + \frac{R_4'}{R_3'}) \)
- First stage \( Q = 1.31 \)
- Second stage \( Q = 0.541 \)
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Fourth Order High Pass Butterworth Filter

- Corner frequency \( f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}} \)
- Passband gain \( H_p = (1 + \frac{R_4}{R_3}) (1 + \frac{R_4'}{R_3'}) \)
- First stage \( Q = 1.31 \)
- Second stage \( Q = 0.541 \)
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10
Typical Applications (Continued)

Ohms to Volts Converter

\[ V_O = \frac{15}{R_{LADD\text{ER}}} \times R_X \]

Where \( R_{LADD\text{ER}} \) is the resistance from switch S1 pole to pin 7 of the TL082CP.
Physical Dimensions  inches (millimeters) unless otherwise noted

Order Number TL082CM
NS Package M08A

Order Number TL082CP
NS Package N08E
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National Semiconductor

Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor
Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 86
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor
Asia Pacific Customer Response Group
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

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