

CLXSA128KA4

Smart Card

DESCRIPTION

The CardLogix CLXSA128KA4 Smart Card incorporates a 262,144 Bit Serial Electrically Erasable PROM in a 32,768 by 8 architecture. This card is for advanced, low power applications such as large record storage and medical applications where low cost per bit is a driving factor.

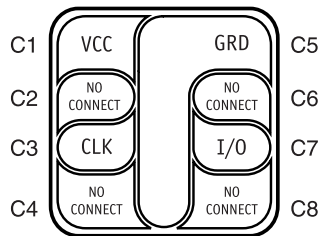
The CLXSA128KA4 offers a straight memory array that features ultra-high-endurance EEPROM for data that changes frequently. The whole array, of 256K bits, is guaranteed at 100,000 ERASE/WRITE (E/W) cycles. The CLXSA128KA4 advanced CMOS technology makes this device ideal for low-power non-volatile data storage applications.

The CLXSA128KA4 is available in the standard ISO 7816, CR80 package or SIM block size.

FEATURES

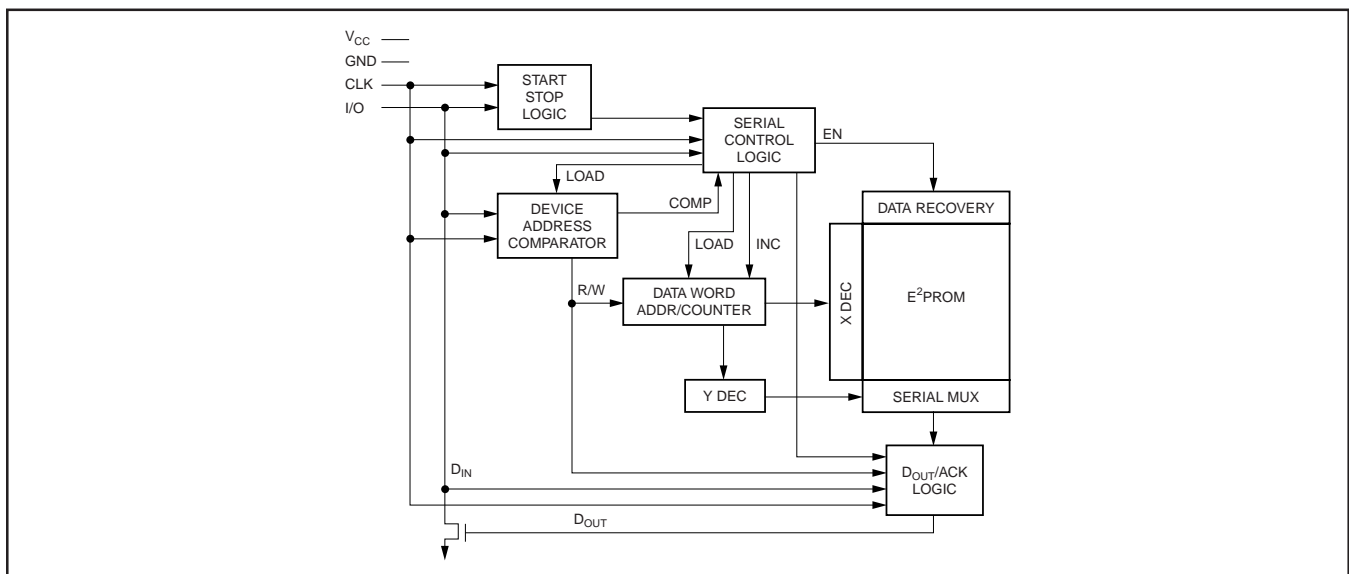
- Voltage operating range: 2.5V to 5.5V
 - Peak write current 3 mA at 5V
 - Maximum read current 1 mA at 5V
 - Standby current 20 μ A typical at 5V
- Industry standard two wire bus protocol
- 64-byte page, or byte modes available
- 1 ms typical write cycle time, byte or page
- Includes 100 khz (2.5V) and 400 khz +1 mhz (5.0V) compatibility
- Filtered inputs for noise suppression
- Power on/off data protection circuitry
- Endurance: >100,000 E/W cycles guaranteed
- Electrostatic discharge protection > 4,000V
- Data retention > 40 years

Typical Module



Card Contacts

BLOCK DIAGRAM



16 Hughes, Suite 100 • Irvine, California 92618 • Ph: (949) 380-1312 • FAX: (949) 380-1428

Preliminary Information: © 1998 CardLogix, Inc. All information is preliminary, and CardLogix retains the right to change and/or withdraw any portion without notice. This document and its contents are covered under U.S. copyright and register laws, all rights reserved.

DCTS-CLXSA128KA4-99c

Page 1

PIN DESCRIPTION

CLOCK (CLK)

The CLK pin is used to positive edge clock data into each card and to negative edge clock data out of the card.

INPUT/OUTPUT (I/O)

The I/O pin is bi-directional for serial data transfer.

RESET (I/O)

the I/O pin is normally pulled high with an external device. Data on the I/O pin may change only during CLK low periods (refer to Data Validity timing diagram). Data changes during CLK high periods will indicate a start or stop condition as defined below.

MEMORY ORGANIZATION

The 128K is internally organized as 512 pages of 64-bytes each. Random word addressing requires a 15-bit data word address.

DEVICE OPERATION

Start Data Transfer

A HIGH to LOW transition of I/O with CLK high is a start condition, which must precede any other command (refer to Start and Stop Definition timing diagram).

Stop Data Transfer

A LOW to HIGH transition of I/O with CLK high is a stop condition. After a read sequence, the stop command will place the E²PROM in a standby power mode (refer to Start and Stop Definition timing diagram).

Acknowledge

All data words are serially transmitted to and from the CLXSA128KA4 in 8-bit words. The card sends a zero during the ninth clock cycle to acknowledge that it has received each word.

Standby Mode The CLXSA128KA4 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

FIGURE 1. BUS TIMING

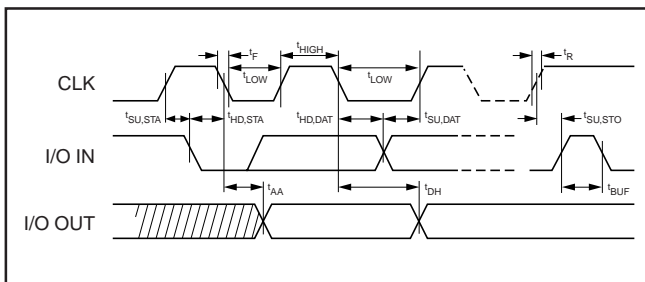


FIGURE 3. DATA VALIDITY

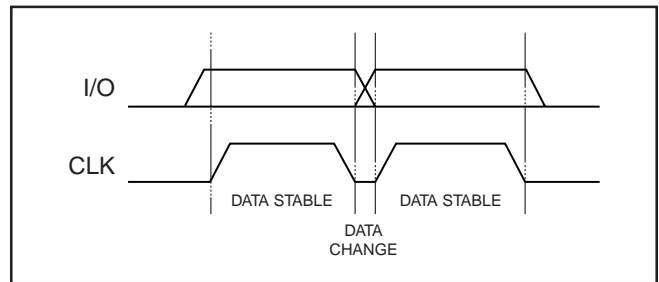


FIGURE 2. WRITE CYCLE TIMING

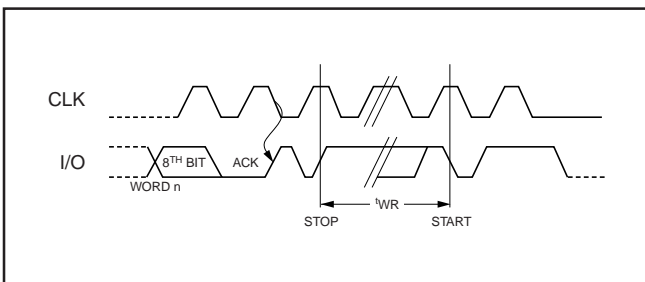


FIGURE 4. START & STOP DEFINITION

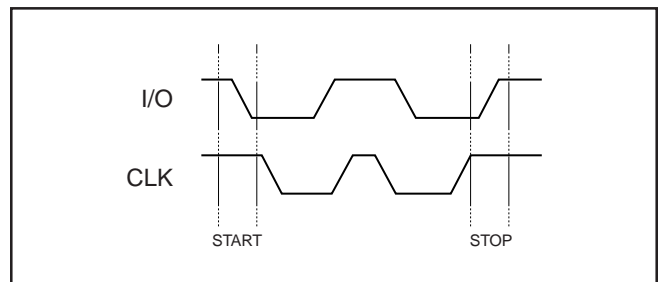
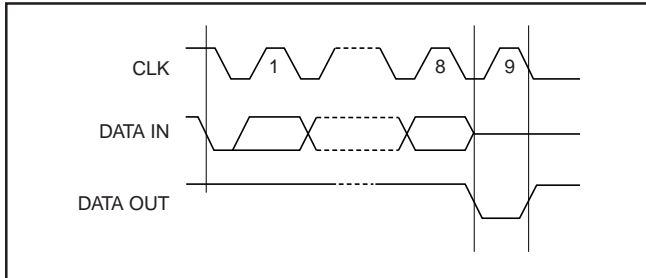


FIGURE 5. OUTPUT ACKNOWLEDGE



DEVICE ADDRESSING

The CLXSA128KA4 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 1). The device address word consists of the bits as shown. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

FIGURE 6. DEVICE ADDRESS

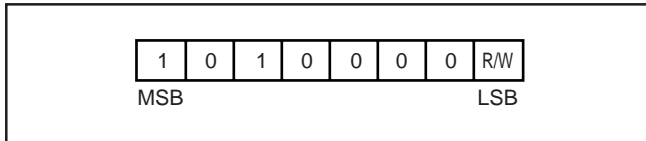


FIGURE 7. BYTE WRITE

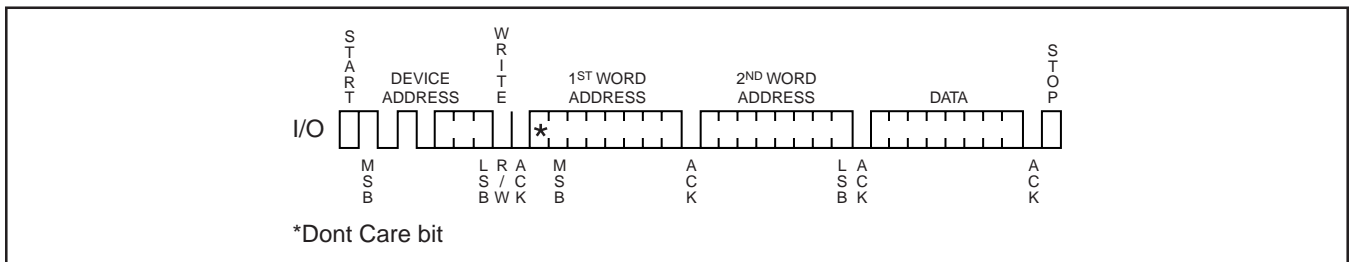
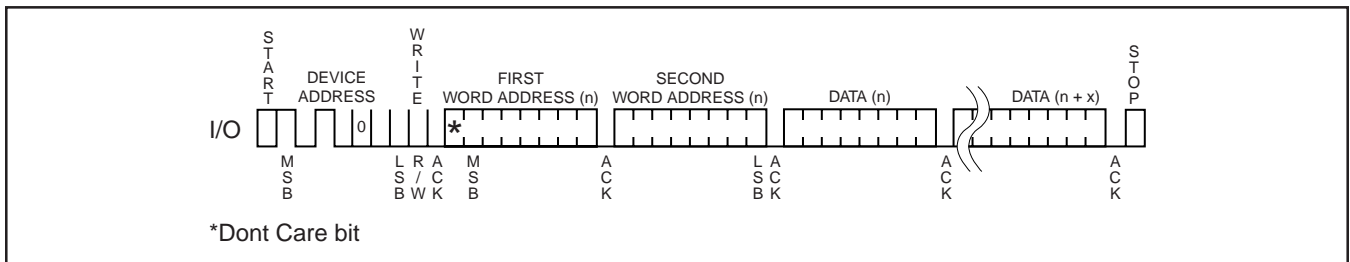


FIGURE 8. PAGE WRITE



BYTE WRITE

A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the card will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the card will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the card enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and the card will not respond until the write is complete (refer to Figure 3).

PAGE WRITE

The CLXSA128KA4 is capable of 64-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first 8 bit data word is clocked in. Instead, after the card acknowledges receipt of the first 8 bit data word, the microcontroller can transmit up to 63 more data words. The card will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 4). The data word address lower 6 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented,

retaining the memory page row location. If more than 64 data words are transmitted to the card, the data word address will “roll over” and previous data will be overwritten. The address “roll over” during write is from the last byte of the current page to the first 8 bit byte of the same page.

ACKNOWLEDGE POLLING

Once the internally-timed write cycle has started and the Card inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the card address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the card respond with a zero, allowing the read or write sequence to continue.

READ OPERATIONS

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the card power is maintained. The address “roll over” during read is from the last byte of the last memory page, to the first byte of the first page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the card, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition.

RANDOM READ

A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the card, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device

FIGURE 9. CURRENT ADDRESS READ

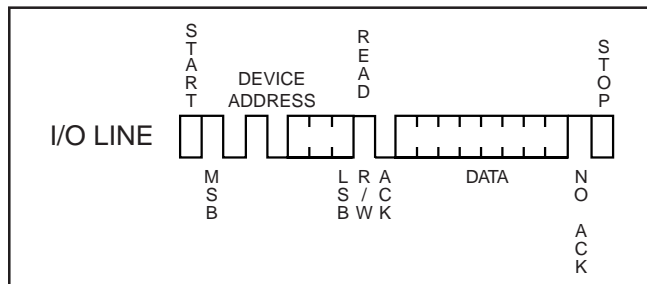
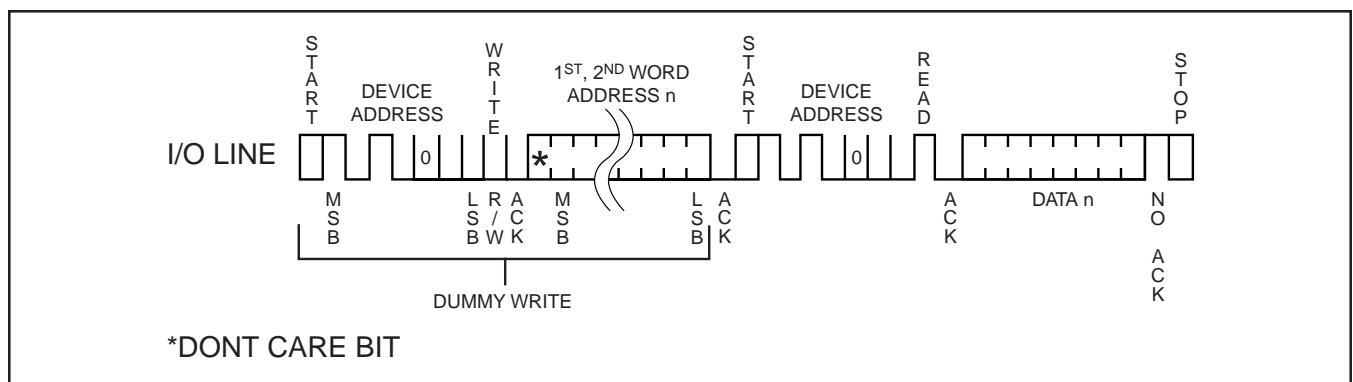


FIGURE 10. RANDOM READ

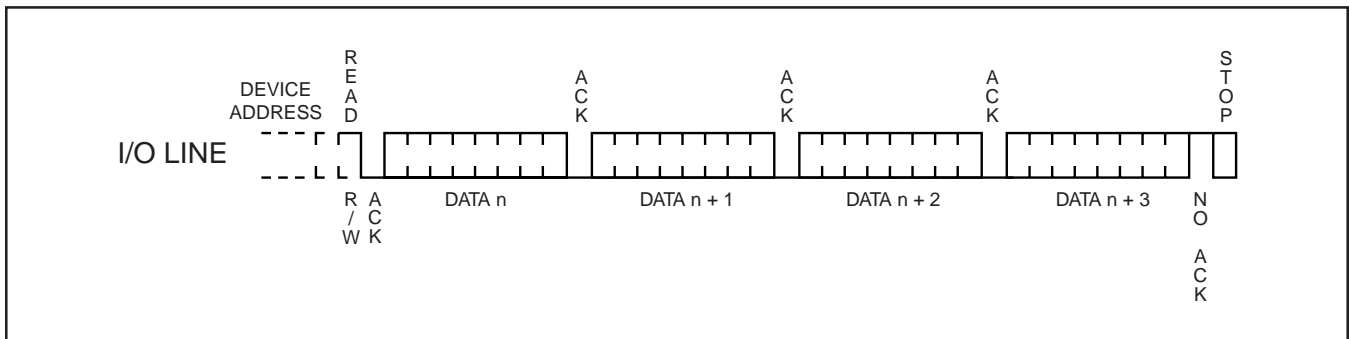


address with the read/write select bit high. The card acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition

SEQUENTIAL READ

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the card receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the reader/writer does not respond with a zero but does generate a following stop condition (refer to Figure 10).

FIGURE 11. SEQUENTIAL READ



AC CHARACTERISTICS

Applicable over recommended operating range from
 TA = -40 °C to +85 °C, VCC = +1.8V to +5.5V, CL = 100 pF
 (unless otherwise noted). Test conditions are listed in Note 2.

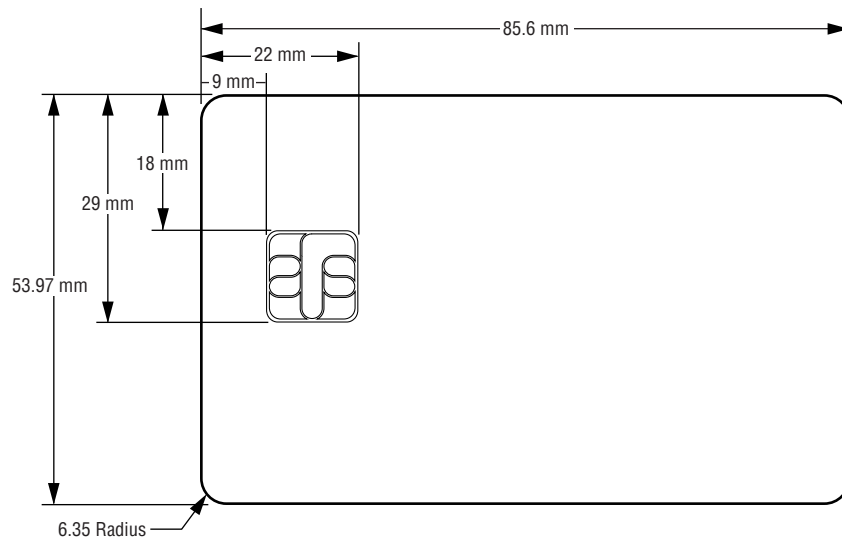
Symbol	Parameter	1.8 Volt		2.7 Volt		5.0 Volt		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLK}	Clock Frequency, CLK		400		1000		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		1.3		0.6		μ s
t_{HIGH}	Clock Pulse Width High	1.0		1.0		0.4		μ s
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	0.1	0.9	0.5	0.55	μ s
t_{BUF}	Time the bus must be free before a new transmission can start	1.2		1.2		0.5		μ s
$t_{HD - STA}$	Start Hold Time	0.6		0.6		0.25		μ s
$t_{SU - STA}$	Start Set-Up Time	0.6		0.6		0.25		μ s
$t_{HD - DAT}$	Data In Hold Time	0		0		0		μ s
$t_{SU - DAT}$	Data In Set-Up Time	100		100		100		ns
t_R	Inputs Rise Time (1)	0.3		0.3		0.3		μ s
t_F	Input Fall Time (1)	300		300		100		ns
$t_{SU - STO}$	Stop Set-Up Time	0.6		0.6		0.25		μ s
t_{DH}	Data Out Hold Time	50		50		50		ns
t_{WR}	Write Cycle Time	10		10		10		μ s

Notes:

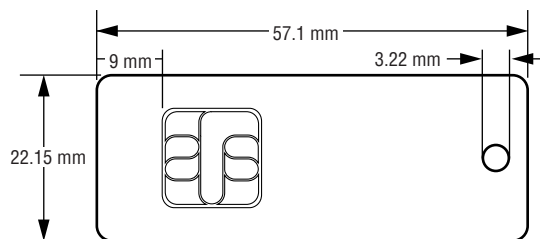
- This parameter is characterized and is not 100% tested.
- AC measurement conditions:
 RL (connects to VCC): 1.3Kohms (2.7V, 5V), 10Kohms (1.8V)
 Input pulse voltages: 0.3VCC to 0.7VCC
 Input rise and fall times: ³ 50ns
 Input and output timing reference voltages: 0.5VCC
 Bus Timing (CLK: Serial Clock, I/O: Serial Data I/O)

CARD DIMENSIONS

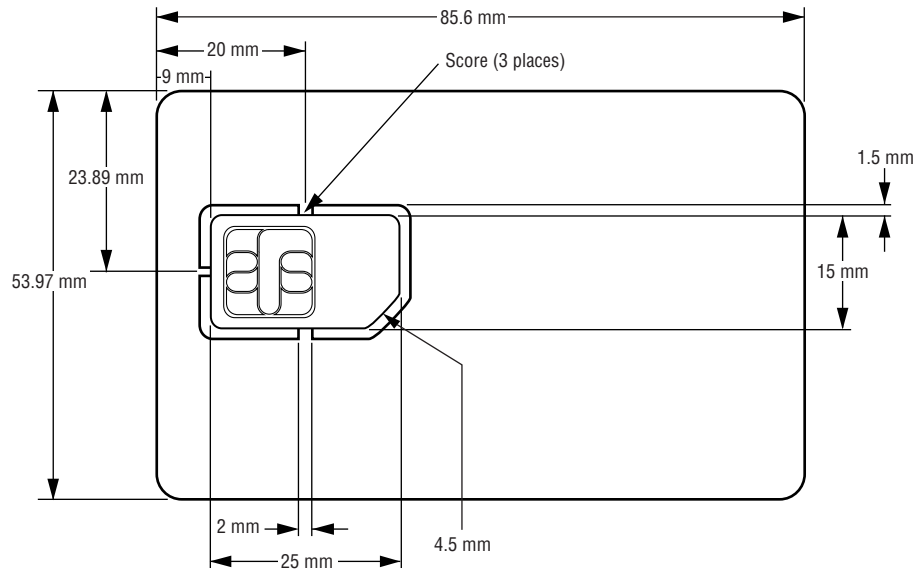
CR80 Smart Card



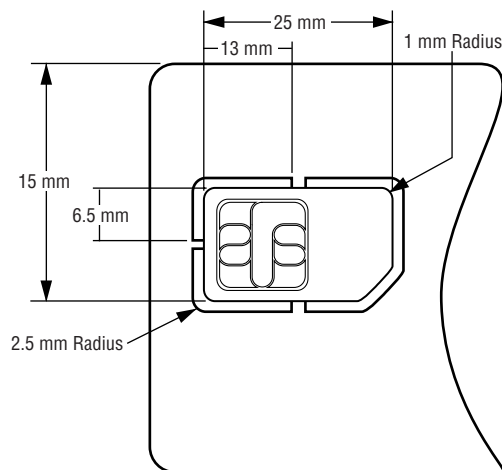
Key Chain Smart Card



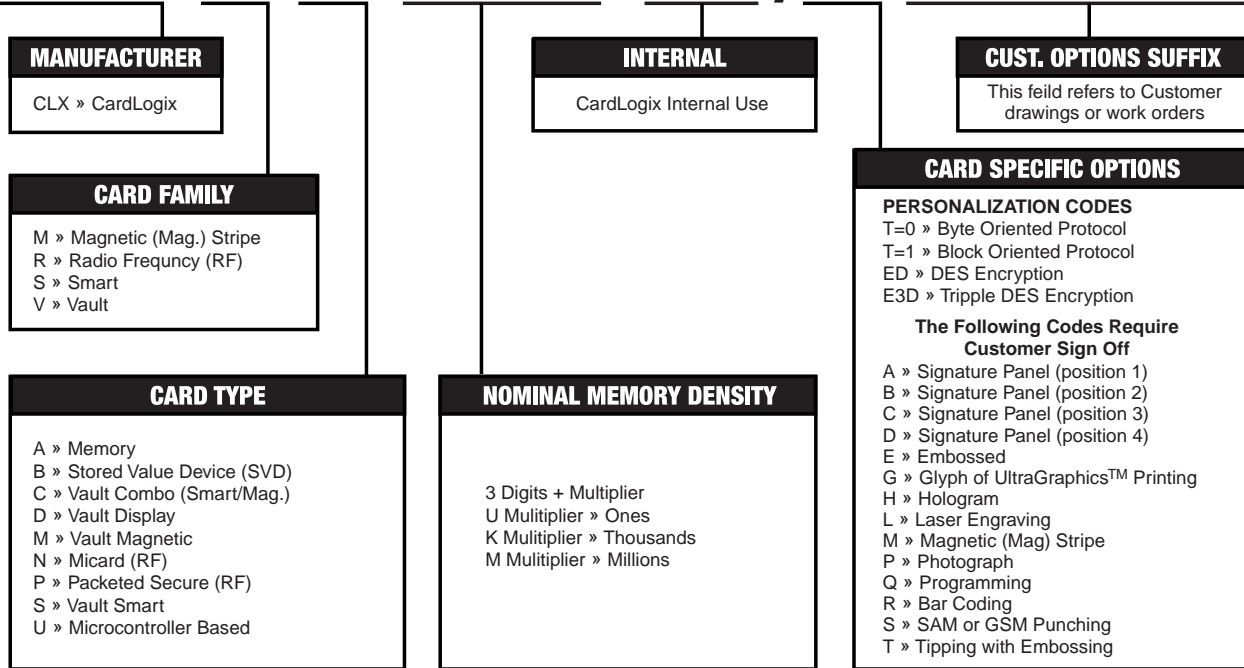
GSM SIM/SAM Smart Card



GSM SIM/SAM Smart Card (Cutout)



CLX S A 128K A4 / X OPTIONS



Quality

CardLogix Corporation is absolutely committed to providing defect free products and services to our customers in partnership with equally committed suppliers and authorized dealers.



Corporate Office (USA)
16 Hughes, Suite 100
Irvine, California 92618

Ph: (949) 380-1312 • Fax: (949) 380-1428

sales@cardlogix.com • <http://www.cardlogix.com> • <http://www.smarttoolz.com>